Modularized Differential Power Processing Architecture Based on Switched Capacitor Converter to Virtually Unify Mismatched Photovoltaic Panel Characteristics

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***Abstract*—Photovoltaic (PV) strings consisting of multiple panels suffer from partial shading or characteristic mismatch issues, such as a significant reduction in power yield. Various kinds of differential power processing (DPP) converters have been developed to prevent the negative impacts of substring-level partial shading. For panel-level applications, however, conventional DPP converters face a variety of challenges, such as impaired extendibility and increased voltage stress of circuit elements. This paper proposes a switched capacitor converter (SCC)-based modular DPP architecture. Modules, each containing series-connected panels with a panel-level DPP converter, are connected through a switchless module-level DPP converter, and PV panel characteristics are unified at module- and panel-levels. The number of panels in each module is fixed, while the number of modules can be arbitrarily extended without redesigning DPP converters, hence offering good modularity. In addition, since voltage stresses of capacitors in the proposed architecture can be reduced lower than half the module voltages, the proposed DPP system realizes all-ceramic-capacitor SCC circuit by properly determining the module voltages. A prototype for eight panels, which were grouped into two modules, was built, and laboratory and field tests were performed. The experimental results demonstrated the enhanced power yield from the partially-shaded PV string.**

Keywords—Differential power processing (DPP) converter, modularization, photovoltaic panel, partial shading, switched capacitor converter.

I. INTRODUCTION

Applications of photovoltaic (PV) panels are rapidly expanding from residential rooftops to solar power plants. Electrical characteristic mismatch of substrings in a PV panel due to partial shading is well known to trigger serious issues. Total energy yield from a PV panel, whose substring characteristics are mismatched, is significantly reduced as a panel current detours through a bypass diode for the weakest substring [1]. In addition, the characteristic mismatch generates multiple power point maxima, including one global and multiple local maximum power points (MPPs), in its *P–V* characteristic curve, confusing ordinally MPP tracking (MPPT) algorithms.

Distributed MPPT systems have been conventionally employed to avoid the partial shading issues. All panels are individually controlled using a module-integrated converter (MIC) or micro-inverters, regardless of characteristic mismatch [2], [3]. Although the energy yield from PV panels can be enhanced thanks to the individual control, increased system cost and complexity are likely because numerous converters in proportion to the number of panels are necessary. Furthermore, since these converters and inverters must process full power of panels, the cost and volume are prone to soar compared to differential power processing converters (DPPs).

To enhance energy yield from PV panels consisting of series-connected substrings, DPP converters or voltage equalizers have been vigorously developed [4]–[31]. A fraction of unshaded substrings' power is transferred to shaded ones through DPP converters so that all substrings operate at the same voltage or even at each MPP, virtually unifying all substring characteristics. Thanks to this power redistribution, local MPPs disappear, and *P–V* characteristic curves of partially-shaded PV panels have only one MPP with enhanced power yield. DPP converters process only differential power, hence contributing to the reduced cost and volume compared to the full power processing MICs and micro-inverters.

In general, to obtain a high voltage, multiple PV panels are connected in series to form a string. Characteristics of series-connected panels are often mismatched due to not only partial shading but also uneven aging, generating the same issues as partial shading. The negative influence of the characteristic mismatch in PV strings can be precluded by DPP converters.

Most conventional DPP converters have been developed aiming for substring level—all substring characteristics in a panel are virtually unified by DPP converters. For panel-level applications, conventional DPP converters face a variety of

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challenges, such as increased collective power conversion loss, impaired extendibility (or modularity), and increased voltage stress of circuit elements, as will be discussed in Section II.

We have proposed the modular DPP architecture based on switched capacitor converters (SCCs) [32], and this paper presents the fully developed work, including detailed operation analysis, derivation of a dc equivalent circuit, and field testing emulating a partial shading condition. Similar to conventional DPP converters and architectures, all panel characteristics are virtually unified in the proposed DPP architecture so that *P–V* characteristics of partially-shaded strings have only one MPP with increased power yield. The proposed modular DPP architecture realizes good extendibility, mitigated voltage stress of circuit elements, and miniaturized circuit at a time.

The rest of this paper is organized as follows. Section II reviews conventional DPP architectures and discusses their benefits and drawbacks. The concept of the proposed modular DPP architecture and its practical circuit implementation will be described in Section III, followed by detailed discussion and comparison on capacitor voltage stresses of SCCs in the conventional and proposed DPP systems in Section IV. Section V derives a dc equivalent circuit, and a design example for two modules, each comprising four panels connected in series, will be presented in Section VI. The dc equivalent circuit-based simulation analysis emulating a partial shading condition will be performed in Section VII. Finally, Section VIII presents the experimental results of the laboratory and field testing for eight panels connected in series under partial shading conditions.

II. Conventional DPP Architectures

In this paper, substring characteristics in each panel are assumed uniform or unified by substring-level DPP converters that are not illustrated for the sake of clarity unless otherwise noted. Conventional DPP converters are roughly categorized into three groups based on power transfer paths: adjacent panel-to-panel, direct panel-to-panel with an isolated port, and string-to-panel DPP converters.

The adjacent panel-to-panel DPP architecture shown in Fig. 1(a) is the most straightforward system. DPP converters transfer power only between adjacent panels so that all panel characteristics are virtually unified. Nonisolated bidirectional PWM converters [4]–[8], multi-stage choppers [9], [10], and some extended topologies of PWM converters [11], [12] are categorized into this architecture. The number of panels in this system can be arbitrarily extended by simply adding panels as well as DPP converters, hence offering good extendibility. A major drawback is the collective power conversion loss due to multiple power conversion stages, which tends to soar with a panel count in a string—for example, power from PV_1 must traverse three DPP converters and two panels before reaching PV_4 in Fig. 1(a), collectively increasing the power conversion loss.

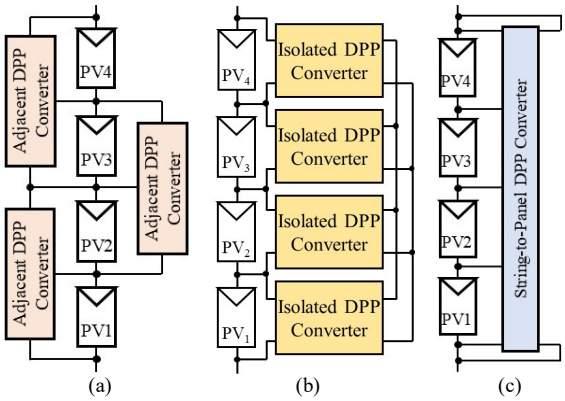

Fig. 1. Conventional DPP architectures: (a) Adjacent panel-to-panel, (b) direct panel-to-panel with isolated port, (c) string-to-panel DPP architectures.

The direct panel-to-panel DPP system with an isolated port [see Fig 1(b)] is based on the use of multiple isolated bidirectional converters [13]–[18]. Although this architecture allows flexible power transfer among panels without suffering from the collective power conversion loss, the need for numerous isolated converters, such as bidirectional flyback converters, is a major drawback as each converter contains at least two switches and a bulky expensive transformer.

A string-to-panel DPP converter used in Fig. 1(c) is essentially a single-input multi-output converter, such as a multi-winding flyback converter [19], multi-stacked buck-boost converters [20], [21], and resonant voltage multipliers [22]–[24]. The number of DPP converters can be reduced to only one, hence simplifying the system and reducing the cost. However, switches with high voltage rating are necessary for the string-to-panel DPP system because switches in these DPP converters must be rated for full string voltage. In addition, since the input voltage of these converters is equal to a string voltage or sum voltage of series-connected panels, these DPP converters need to be redesigned when the number of panels changes. In other words, poor extendibility is a drawback of this DPP system.

III. Proposed Modular DPP Architecture Based on Switched Capacitor Converters

A. Switched Capacitor Converters

The proposed modular DPP architecture is based on modularized SCCs. Although a variety of SCCs have been developed as DPP converters [25]–[31], two SCC topologies shown in Fig. 2 can be used as DPP converters for series-connected PV panels. High- and low-side switches in both topologies operate with a fixed 50% duty cycle in a complementary mode.

The ladder-type SCC shown in Fig. 2(a) is one of the most popular adjacent panel-to-panel DPP converters. Voltage ratings of switches and capacitors are equal to a panel voltage V_{PV}. The number of panels connected in series can be arbitrarily extended by simply stacking switches and capacitors, offering good modularity (or extendibility). However, power transfer is limited only between adjacent panels, and hence, power conversion loss would become collectively soar in the course of multiple power conversions. Power from PV_1, for instance, has to be transferred via C_1–C_3 before reaching PV_4. The collective power conversion loss would be even significant in high-voltage strings comprising numerous panels connected in series.

Meanwhile, the SCC shown in Fig. 2(b) [33], [34] is

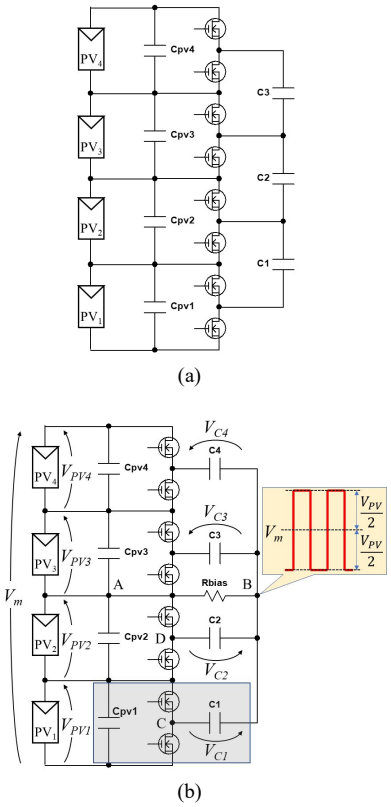

Fig. 2. Switched capacitor converters for (a) adjacent panel-to-panel DPP converter and (b) nonisolated direct panel-to-panel DPP converter.

equivalent to a nonisolated direct panel-to-panel DPP converter. Since all capacitors are connected to the common node of B in this topology, the bias resistor R_{bias} is used to stabilize capacitor voltages—a small bias current of a few milliamperes for R_{bias} would be sufficient to stabilize the voltage at node B. Power can be transferred between any two panels through two capacitors. For example, power from PV_1 can reach PV_4 through only C_1 and C_4, reducing the power conversion stages compared to the ladder-type SCC shown in Fig. 2(a).

Although this direct power transfer realizes relatively efficient power conversion, voltage stresses of capacitors tend to increase with the number of panels. Voltage stresses of C_1 and C_2 are briefly determined as an example. The average potential at node B is equal to that of node A thanks to R_{bias}. Average potentials at nodes C and D are $V_{PV}/2$ and $3V_{PV}/2$ (V_{PV} being an equalized panel voltage), respectively, because switches operate with 50% duty cycle. Hence, average voltages of C_1 and C_2 are determined to be $3V_{PV}/2$ and $V_{PV}/2$, respectively.

This tendency suggests that voltage stresses of outer capacitors (i.e., C_1 and C_4), which are distally-placed from the middle point B, are high, and vice versa for inner capacitors (i.e., C_2 and C_3). In addition, since capacitor voltages soar as the number of panels grows, reselection for capacitors is unavoidable for strings comprising a larger number of panels. Thus, the number of panels cannot be readily changed with this SCC, impairing the modularity of the system.

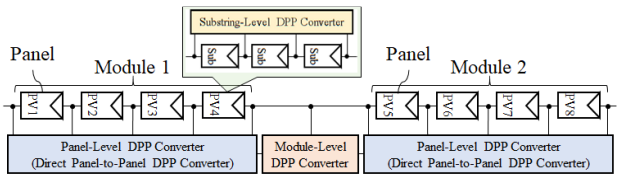

Fig. 3. Notional schematic diagram of proposed modular DPP architecture.

B. Proposed Modular DPP Architecture

The notional schematic diagram of the proposed modular DPP architecture is illustrated in Fig. 3. In this example, four panels are grouped as a module having a panel-level DPP converter. Panel-level DPP converters are connected through a module-level DPP converter. It is noted again that this paper focuses on panel- and module-level DPP converters, and substring characteristics in each panel are assumed uniform or unified by substring-level DPP converters, as shown in the inset of Fig. 3.

Characteristic mismatch in each module (i.e., the mismatch in panel characteristics) is efficiently eliminated by each panel-level DPP converter, whereas the module-level DPP converter transfers power between two adjacent modules so that characteristic mismatch between modules is eliminated. In other words, PV panels in the modular architecture are unified at two levels—module and panel levels.

The practical implementation of the proposed modular DPP architecture is shown in Fig. 4. Each panel-level DPP converter employs the nonisolated direct panel-to-panel SCC shown in Fig. 2(b) that operates with a fixed 50% duty cycle. The module-level DPP converter, on the other hand, is a switchless topology consisting of two capacitors (C_a and C_b) and one inductor L. C_a and C_b are connected in series in order to halve their voltage stress, and their voltages are equalized by L at 50%

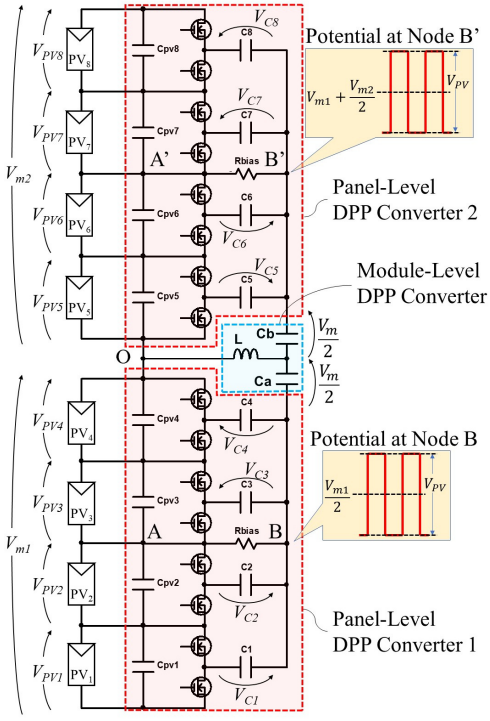

Fig. 4. Proposed SCC-based modular DPP architecture.

duty cycle operation. The halved voltage stress of C_a and C_b realizes all-ceramic-capacitor circuit—if not halved, the voltage stress of capacitors might be as high as a full module voltage, and bulky film capacitors with high voltage rating would be necessary. Although one inductor is necessary for a module-level DPP converter, a small inductor with low current rating suffices because of a small bias current under steady-state conditions.

C. Major Features

Similar to conventional SCC-based topologies [25], [26], [33], [34] the proposed modular DPP architecture operates with a fixed 50% duty cycle. Thus, no feedback control loop is necessary, allowing simplified circuit and ease of design.

The most prominent features of the modular DPP architecture are the improved modularity and decreased voltage stress of capacitors. The number of panels in each module is fixed (e.g., four panels), while the number of modules can be arbitrary extended with simply stacking modules with module-level DPP converters. Voltage stresses of capacitors in the proposed modular DPP architecture are lower than half the module voltage, not a string voltage. Hence, capacitor voltage rating can be rather lower than the string voltage, allowing high-energy-density multi-layer ceramic capacitors (MLCCs) with relatively low-voltage rating to be employed.

In contrast, with the conventional DPP converters of the SCC shown in Fig. 2(b), the number of panels might be arbitrary extended with adding as many capacitors and switches as needed, whereas voltage stresses of capacitors are dependent on a string voltage. In other words, voltage stresses of capacitors soar with the string voltage, and bulky film capacitors with high-voltage rating would likely be required. Furthermore, the conventional DPP converters must be redesigned by reselecting capacitors with proper voltage rating when the number of panels changes. Detailed analysis and comparison on capacitor voltage stress will be performed in the next section.

MPP voltages vary slightly with irradiance and strongly with temperatures. In the proposed DPP architecture, panel and module voltages are automatically equalized, similar to conventional SCC-based DPP converters. Individual MPPT operations by DPP converters proposed in [7]–[10] would achieve greater energy yield from PV strings at the cost of complex control techniques. However, previous works [8], [14], [15] reported that the difference between the individual MPPT and voltage equalization is merely around 2% chiefly because MPP voltages are insensitive to shading conditions [25]. Hence, the proposed DPP architecture is expected to adequately improve energy yield under partial shading conditions by simply equalization voltages.

IV. Capacitor Voltage Stress

A. Voltage Stress of Capacitors in Panel-Level DPP Converter

The topology of the panel-level DPP converter is identical to that of the SCC shown in Fig. 2(b), and so are the voltage stresses of capacitors, as discussed in Section III-A. Voltage rating necessary for capacitors soars with the number of panels connected in series in a module. The number of panels in a module should be chosen so that small compact MLCCs can be used for the SCC. This paper deals with the case of four panels in each module.

B. Voltage Stress of Capacitors in Switchless Module-Level DPP Converter

The fundamental operation of the module-level DPP converter is very similar to that of the conventional adjacent panel-to-panel DPP converter shown in Fig. 2(a). Thus, before detailing the operation of the module-level DPP converter, we discuss the SCC shown in Fig. 2(a).

A unit circuit of the conventional SCC is shown in Fig. 5(a). As the odd- and even-numbered switches are alternately driven with a fixed 50% duty cycle, square wave voltages are generated across Q_2 and Q_3 in the form of v_{Q2} and v_{Q3}, respectively, which are 180° out of phase. With v_{Q2} and v_{Q3}, the unit SCC circuit can be expressed using the equivalent circuit shown in Fig. 5(b). Peak-to-peak voltages of v_{Q2} and v_{Q3} are V_{m1} and V_{m2}, and their average voltages are $V_{m1}/2$ and $V_{m2}/2$, respectively, because of the 50% duty cycle operation. Hence, the average voltage of C_A is equal to the sum of the averages of V_{m1} and V_{m2} [i.e., $(V_{m1}+V_{m2})/2$].

Similar to the conventional unit SCC of Fig. 5(b), an equivalent circuit of the switchless module-level DPP converter is illustrated in Fig. 6. Square wave voltage sources, v_{OB} and $v_{B'O}$, correspond to the voltages across nodes O–B and B'–O, respectively (see Fig. 4). Their average voltages are $V_{m1}/2$ and $V_{m2}/2$, respectively. Since an average voltage of L must be zero under steady-state conditions, the average voltages of C_a and C_b are $V_{m1}/2$ and $V_{m2}/2$.

Assuming the ideal case, all the module voltages are unified to be V_m. In comparison between the conventional SCC [Fig. 5(a)] and proposed module-level DPP converter (Fig. 6), the voltage stress of C_a and C_b in the proposed DPP converter is half that of the conventional SCC. For example, for modules

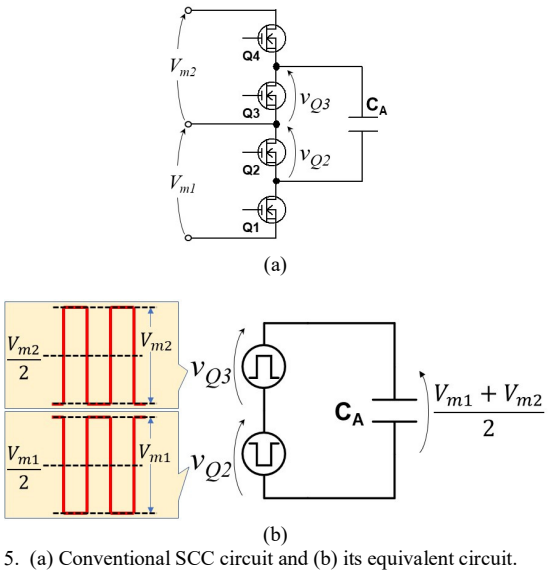

Fig. 5. (a) Conventional SCC circuit and (b) its equivalent circuit.

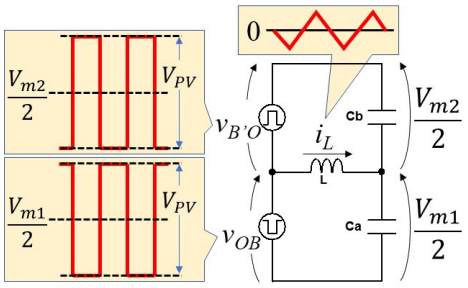

Fig. 6. Equivalent circuit of module-level DPP converter.

comprising four standard 72-cell panels, each with approximately 45 V open circuit voltage, the voltage of C_a in the conventional SCC reaches 180 V, and a bulky film capacitor would be necessary to withstand such high voltage stress. With the proposed module-level DPP converter, on the other hand, voltage stresses of C_a and C_b can be halved to 90 V, allowing compact MLCCs to be employed. Although an additional inductor is necessary to equally divide voltages across C_a and C_b, its volume impact is very minor. Since L is tied to the middle point of two capacitors, its average current is zero under steady-state conditions. Hence, a small inductor with a low current rating can be employed.

C. Comparison

All panel voltages are assumed to be equalized as 36 V in this comparison. In other words, the module voltages in the modular DPP system are 144 V. Voltage stresses of capacitors in the conventional nonisolated direct panel-to-panel DPP converter for eight panels connected in series (Fig. 7) and proposed modular DPP system (Fig. 4) are compared in Table I. Voltage stresses of outer capacitors of C_1 and C_8 in the conventional DPP converter are the highest, while those of inner capacitors of C_4 and C_5 are low. This tendency is also true in each panel-level DPP converter in the proposed modular DPP system; outer capacitors in each panel-level DPP converter (C_1 and C_4 in Module 1, and C_5 and C_8 in Module 2) are exposed to relatively high voltage stress. However, their voltage stress is rather lower than that in the conventional DPP converter thanks to C_a and C_b in the switchless module-level DPP converter.

Outer capacitors in the conventional direct panel-to-panel DPP converter are exposed to high voltage stress of 126 V (see Table I), and hence, bulky film capacitors are likely necessary. In the proposed modular DPP system, on the other hand, all capacitor voltage stresses are lower than 72 V (half the module voltage). The reduced voltage stresses allow all-MLCC circuit, achieving miniaturized circuit design.

V. DC Equivalent Circuit

Simulation-based analysis for PV strings employing an MPPT algorithm takes a long stretch of time because of the huge difference between switching period and MPPT sampling interval—switching periods are around 10 μs (equivalent to 100-kHz switching frequency), whereas sampling intervals can be longer than hundreds of milliseconds. To reduce the simulation burden and time, a dc equivalent circuit is derived in this section. The dc equivalent circuit is simpler and contains no high-frequency operation, hence significantly mitigating the simulation burden.

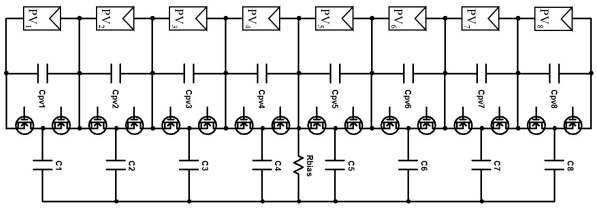

Fig. 7. Conventional nonisolated direct panel-to-panel DPP converter for eight panels.

TABLE I
VOLTAGE STRESS OF CAPACITORS

Capacitor	Conventional	Proposed
C_1	126 V	54 V
C_2	90 V	18 V
C_3	54 V	18 V
C_4	18 V	54 V
C_5	18 V	54 V
C_6	54 V	18 V
C_7	90 V	18 V
C_8	126 V	54 V
C_a, C_b	—	72 V

A. Equivalent Resistance of SCC

In general, charge and discharge of a capacitor in SCCs can be equivalently expressed as an equivalent resistance that is inversely proportional to capacitance and frequency. A basic unit SCC circuit shown in Fig. 5(a) can be transformed into a dc equivalent circuit shown in Fig. 8 [35], in which the current $I_{eq.i}$ flows through the equivalent resistor $R_{eq.i}$ and an ideal transformer between two voltage sources, V_{m1} and V_{m2}. The value of $R_{eq.i}$ [36] is given by

$$R_{eq.i} = \frac{V_{m1} - V_{m2}}{I_{eq.i}} = \frac{1}{Cf_s} \frac{exp\left(\frac{T}{\tau}\right) - 1}{\left\{exp\left(\frac{dT}{\tau}\right) - 1\right\}\left\{exp\left(\frac{(1-d)T}{\tau}\right) - 1\right\}} \quad (1)$$

where C is the capacitance, f_S (= $1/T$) is the switching frequency, d is the duty cycle, and τ is the time constant of capacitors. It is noteworthy that, in the panel-level DPP converter, C_i together with switches and a smoothing capacitor C_{pvi} [as highlighted with grey in Fig. 2(b)] can be modeled as $R_{eq.i}$ because a current of C_i flows through a switch and C_{pvi}, as shown in Fig. 9, in which current flow directions under the case that PV_2 is shaded. Focusing on circuit elements corresponding to PV_1 (i.e., C_1, C_{pv1}, Q_{1L}, and Q_{1H}), C_1 and C_{pv1} are connected in series through Q_{1L} during Mode A [see Fig. 9(a)], whereas C_1 discharges alone through Q_{1H} in Mode B [see Fig. 9(b)]. Hence, the combined

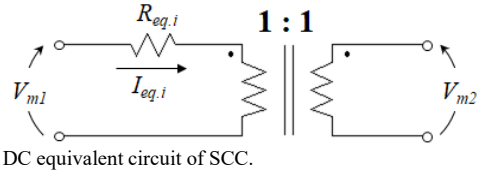

Fig. 8. DC equivalent circuit of SCC.

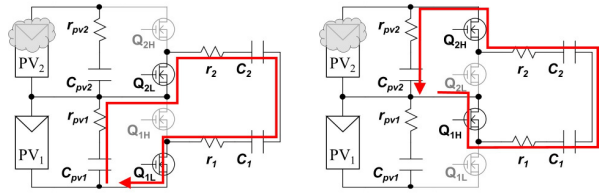

Fig. 9. Current flow paths in (a) Mode A and (b) Mode B.

resistance and capacitance over a single switching cycle are (R_{on} + r_i + r_{pvi}/2) and $C_1 \| 2C_{pv1}$, respectively (where R_{on} is the on-resistance of switches, r_i and r_{pvi} are the ESR of C_1 and C_{pv1}, respectively — r_{pvi}/2 and $2C_{pv1}$ represent that C_{pv1} is connected in series with C_1 only for half the switching period. Meanwhile, C_i in the module-level DPP converter can be modeled independently on switches and C_{pvi}. Hence, C and τ in (1) are given by

$$C = \begin{cases} \dfrac{2C_iC_{pvi}}{C_i + 2C_{pvi}} & (i = 1 \cdots 8) \\ C_i & (i = a \text{ or } b) \end{cases}$$
$$\tau = \begin{cases} \left(\dfrac{2C_iC_{pvi}}{C_i + 2C_{pvi}}\right)\left(R_{on} + r_i + \dfrac{r_{pvi}}{2}\right) & (i = 1 \cdots 8) \\ C_i r_i & (i = a \text{ or } b) \end{cases} \quad (2)$$

B. DC Equivalent Circuit

By transforming all capacitors into equivalent resistors (see Fig. 8), the dc equivalent circuit of the proposed modular DPP system can be derived as shown in Fig. 10. PV panels in each module are virtually connected in parallel through respective $R_{eq.i}$ and an ideal multi-winding transformer. Meanwhile, the module-level DPP converter can also be expressed using $R_{eq.a}$ and $R_{eq.b}$ that represents C_a and C_b. Overall, all panels are virtually connected in parallel through $R_{eq.i}$, and therefore, their voltages are automatically nearly unified as long as voltage drops across $R_{eq.i}$ are satisfactory small.

This dc equivalent circuit contains no switching device operating at a high frequency, and therefore, the simulation time and burden can be greatly reduced in comparison with the original circuit shown in Fig. 4. However, the dc equivalent circuit is not suitable for analyzing dynamic response characteristics because it represents behaviors under steady-state conditions.

An individual panel current I_i (i = 1…8) can be expressed as

$$I_i = I_{ave.k} + \Delta I_i \quad (3)$$

where $I_{ave.k}$ is the average of I_i in Module k (k = 1 or 2), and ΔI_i is the deviation of I_i from $I_{ave.k}$. The string current, I_{st}, is the sum of I_i and equalization current $I_{eq.i}$. From (3),

$$I_{st} = I_i + I_{eq.i} = I_{ave.k} + \Delta I_i + I_{eq.i} \quad (4)$$

This equation suggests that $I_{eq.i}$ increases with the current mismatch among panels (i.e., ΔI_i). According to the equivalent circuits (Figs. 8 and 10) and (1), large $I_{eq.i}$ is prone to large voltage imbalance among panels due to a voltage drop across $R_{eq.i}$. Hence, the value of $R_{eq.i}$ [or the value of C in (1) and (2)] should be properly determined considering the largest expected

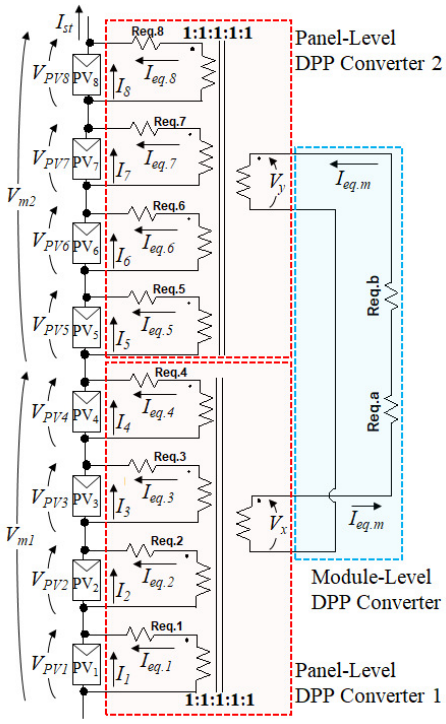

Fig. 10. DC equivalent circuit of proposed modular DPP system for eight panels.

$I_{eq.i}$ so that voltage imbalance is within an acceptable range, as will be exemplified in Section VI.

Kirchhoff's current law in each module gives

$$\sum_{i=1}^{4} I_{eq.i} + I_{eq.m} = 0, \qquad \sum_{i=5}^{8} I_{eq.i} - I_{eq.m} = 0 \quad (5)$$

where $I_{eq.m}$ is the module's equalization current. Substitution of (4) into (5) produces

$$I_{st} = \begin{cases} I_{ave.1} + \dfrac{1}{4}\displaystyle\sum_{i=1}^{4}(\Delta I_i + I_{eq.i}) = I_{ave.1} - \dfrac{I_{eq.m}}{4} \\ I_{ave.2} + \dfrac{1}{4}\displaystyle\sum_{i=5}^{8}(\Delta I_i + I_{eq.i}) = I_{ave.2} + \dfrac{I_{eq.m}}{4} \end{cases} \quad (6)$$

where $I_{ave.1}$ and $I_{ave.2}$ are the averages of I_i in Modules 1 and 2, respectively. Substituting (6) into (4) yields

$$I_{eq.i} = \begin{cases} I_{ave1} - I_i - \dfrac{I_{eq.m}}{4} \\ I_{ave2} - I_i + \dfrac{I_{eq.m}}{4} \end{cases} \quad (7)$$

Rearrangement of (7) yields $I_{eq.m}$ as

$$I_{eq.m} = 2(I_{ave.1} - I_{ave.2}) \quad (8)$$

This equation indicates that the difference between $I_{ave.1}$ and $I_{ave.2}$ flows through the module-level DPP converter, and the current rating of the module-level DPP converter needs to be determined with considering the largest expected $I_{eq.m}$. One whole module might be completely shaded in the worst case,

but this is very unlikely and infrequent as long as PV panels are properly installed considering the surrounding environment. The current rating of the module-level DPP converter should desirably be determined depending on applications and the surrounding environment.

C. Voltage Imbalance due to Equivalent Resistance

PV panels generating the highest and lowest currents (I_H and I_L) in a module are defined as PV_H and PV_L, respectively, and their equalization currents are $I_{eq.H}$ and $I_{eq.L}$. From Ohm's law in Fig. 10, the maximum voltage difference in a module, ΔV_{max}, is given by

$$\Delta V_{max} = V_{PV.H} - V_{PV.L} = -I_{eq.H}R_{eq.H} + I_{eq.L}R_{eq.L} \quad (9)$$

where $R_{eq.H}$ and $R_{eq.L}$ are the equivalent resistors corresponding to PV_H and PV_L, respectively. By assuming $R_{eq.H} = R_{eq.L} = R_{eq}$, (9) can be simplified to be

$$\Delta V_{max} \approx R_{eq}\left(-I_{eq.H} + I_{eq.L}\right) = R_{eq}(I_H - I_L) \quad (10)$$

This equation does not contain $I_{eq.m}$, suggesting that ΔV_{max} is not dependent on module equalization. It should be noted that R_{eq} in practical use varies depending on positions because capacitances of MLCCs are dependent on bias voltages.

Module voltages V_{m1} and V_{m2} are expressed as

$$\begin{cases} V_{m1} = \sum_{i=1}^{4} V_{PVi} = 4V_x - \sum_{i=1}^{4} I_{eq.i}R_{eq.i} \\ V_{m2} = \sum_{i=5}^{8} V_{PVi} = 4V_y - \sum_{i=5}^{8} I_{eq.i}R_{eq.i} \end{cases} \quad (11)$$

where V_x and V_y are the winding voltages in Modules 1 and 2, respectively, as designated in Fig. 9.

The relationship between V_x and V_y is

$$V_x - V_y = I_{eq.m}\left(R_{eq.a} + R_{eq.b}\right) \quad (12)$$

From (5), (11), and (12) with assuming $R_{eq.i} = R_{eq}$ and $R_{eq.a} = R_{eq.b} = R_{eq.m}$, the voltage difference between modules, ΔV_m, is yielded as

$$\Delta V_m = V_{m1} - V_{m2} = I_{eq.m}\left(8R_{eq.m} + 2R_{eq}\right) \quad (13)$$

This equation suggests that ΔV_m is dependent on not only the module-level DPP converter (i.e., $R_{eq.m}$) but also the panel level DPP converter (i.e., R_{eq}).

VI. Design Example

This section presents a design example for a PV string consisting of two modules each containing four panels connected in series. 60- or 72-cell monocrystalline PV panels with a short-circuit current of I_{sc} = 6.0 A, open-circuit voltage of V_{oc} = 45 V, and maximum power point voltage of V_{mp} = 36 V are considered.

A. Design Guideline

The previous work compared the energy yield between individual MPPT capability and voltage equalization [8], [14], [15]. Although voltage equalization does not ensure all panels operate at each MPP, the loss in energy yield is reportedly less than a few percent in comparison with individual MPPT. The proposed modular DPP system is categorized into voltage equalizers, but panel voltages cannot be perfectly equalized due to voltage drops across equivalent resistors (R_{eq}), as can be seen in Fig. 10. To suppress the voltage drops low enough for satisfactory voltage equalization, the equivalent resistance R_{eq} needs to be properly determined with considering the equalization currents $I_{eq.i}$. Previous works [37], [38] concluded that DPP converters capable of processing 20–30% of panels' maximum power can satisfactorily preclude the mismatch issues in most practical situations.

In this section, a prototype of the proposed modular DPP system is designed for the following mismatch conditions and voltage equalization target:

- ✓ The largest current mismatch in each module (i.e., $I_H - I_L$) is 1.5 A, which corresponds to approximately 25% of the short-circuit current
- ✓ The largest current mismatch between modules (i.e., $I_{ave.1} - I_{ave2}$) is 0.5 A
- ✓ The maximum voltage difference in each module ΔV_{max} is less than 5% at the maximum power voltage of the panels of 144 V (= 36 V × 4)
- ✓ The maximum voltage difference between modules is less than 5% of the maximum power voltage of the modules

B. Determination of Equivalent Resistance and Capacitance

For the sake of design simplicity, all equivalent resistances of $R_{eq.i}$ are assumed identical. For ΔV_{max} to be less than 5% of V_{mp} = 36 V, $R_{eq.i}$ can be obtained from (10), as

$$R_{eq} \le \frac{\Delta V_{max}}{I_H - I_L} = \frac{36V \times 0.05}{1.5A} = 0.90\ \Omega \quad (14)$$

Similarly, given $I_{ave.1} - I_{ave2}$ = 0.5 A and ΔV_{max} less than 5% of 144 V, $R_{eq.m}$ is determined based on (13) with substituting (8), as

$$R_{eq.m} \le \frac{\Delta V_m}{8 \times 2(I_{ave.1} - I_{ave.2})} - \frac{R_{eq}}{4} = \frac{144V \times 0.05}{8 \times 1A} - \frac{R_{eq}}{4} = 0.90\ \Omega - \frac{R_{eq}}{4} \quad (15)$$

Assuming $R_{eq.m} = R_{eq}$,

$$R_{eq.m} = R_{eq} \le 0.72\ \Omega \quad (16)$$

Assuming r_i = 5 mΩ and r_{on} = 36 mΩ, capacitances required to fulfill (16) can be calculated to be approximately 14 μF, according to (2). In general, a capacitance of MLCCs is dependent on a bias voltage. C_a and C_b in the module-level DPP converter are exposed to higher voltages than C_i in the panel-level DPP converters. Given the reduced capacitances at the

TABLE II
BIAS VOLTAGE AND EQUIVALENT RESISTANCE VALUES

Capacitor	Bias Voltage	Capacitance at Bias Voltage	$R_{eq.i}$
C_1, C_4, C_5, C_8	54 V	18.5 μF (= 3.7 μF×5)	0.69 Ω
C_2, C_3, C_6, C_7	18 V	42.5 μF (= 8.5 μF×5)	0.45 Ω
C_a, C_b	72 V	26.0 μF (= 2.6 μF×10)	0.48 Ω
C_{pv1}–C_{pv8}	36 V	42.9 μF (= 14.3 μF×3)	—

high bias voltage, five or ten 10-µF MLCCs with 100-V rating (CGA9N3X7S2A106K230KB, TDK) were selected for C_1–C_8, C_a, and C_b. For smoothing capacitors of C_{PV1}–C_{PV8}, three 22-µF MLCCs (KCM55WR71H226MH01, Murata) were employed.

The bias voltage, actual capacitance, and calculated $R_{eq.i}$ values are listed in Table II. Values of $R_{eq.i}$ vary depending on the bias voltage chiefly because same MLCCs were selected for C_1–C_8, C_a, and C_b. Values of $R_{eq.i}$ might be optimally designed by properly selecting MLCCs depending on bias voltages, but it complicates the design procedure and component selection.

VII. Simulation Results

A simulation test based on PSIM software was performed using the dc equivalent circuit shown in Fig. 10 with assuming that standard 72-cell monocrystalline PV panels were employed. The values of $R_{eq.i}$ in Table II, which have been calculated considering the reduced capacitance due to a bias voltage, were used for the simulation. PV panel characteristics were emulated using look-up tables.

Individual panel characteristics used for the simulation are shown in Figs. 11(a). In addition to the mismatched panel characteristics in each module, module characteristics were also

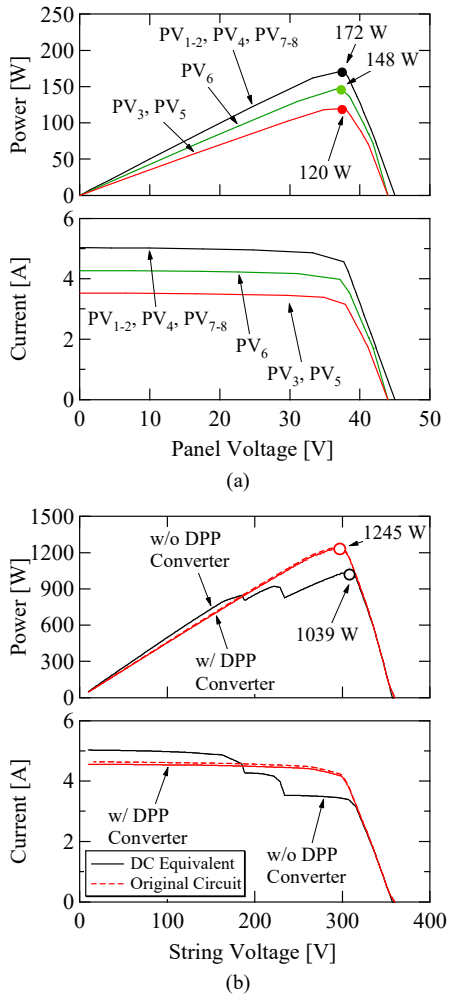

Fig. 11. Simulation results: (a) individual panel characteristics, (b) String characteristics with/without modular DPP system.

TABLE III
Individual Panel Voltages When String Operated at MPP in Simulation

Panel	Voltage
PV_1	37.7
PV_2	37.8
PV_3	36.9
PV_4	37.7
PV_5	36.8
PV_6	37.1
PV_7	37.5
PV_8	37.5

mismatched in order to verify the performance of the proposed modular DPP system—one panel in Modules A (PV_3) and two panels in Module B (PV_5 and PV_6) were mismatched, respectively.

Measured string characteristics with/without the DPP system are shown and compared in Fig. 11(b). Without the DPP system, two power point maxima, including one global and two local MPPs, were observed, and its extractable maximum power was merely 1039 W. With the DPP system, on the other hand, the local MPP vanished, and the maximum power increased to as high as 1245 W, corresponding to 19.8% improvement. Characteristics of the original circuit (Fig. 4) and dc equivalent circuit (Fig. 10) matched very well, verifying the derived dc equivalent circuit and its equivalent resistance model.

Individual panel voltages when the string operated at the MPP with the DPP system are shown in Table III. The maximum voltage differences ΔV_{max} in Modules 1 and 2 were 0.9 and 0.7 V, respectively, and the module voltage difference ΔV_m was 1.2 V. All the panels and modules were equalized well with minor residual voltage mismatch observed, verifying the sufficient voltage equalization capability of the proposed DPP system.

VIII. Experimental Results

A. Prototype

A prototype of the proposed modular SCC-based DPP

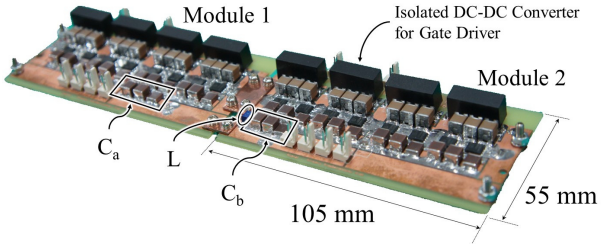

Fig. 12. Prototype of modular DPP system for two modules, each comprising four panels.

TABLE IV
Component List

Component	Value
C_{pv1}–C_{pv8}	MLCC (KCM55WR71H226MH01), 22 µF × 3, 50 V
C_1–C_8	MLCC (KRM55TR72A106MH01K), 10 µF × 5, 100 V
C_a, C_b	MLCC (KRM55TR72A106MH01K), 10 µF × 10, 100 V
L	1 mH
MOSFET	BSC320N20NS3G, R_{on} = 36 mΩ
Gate Driver	IR2184

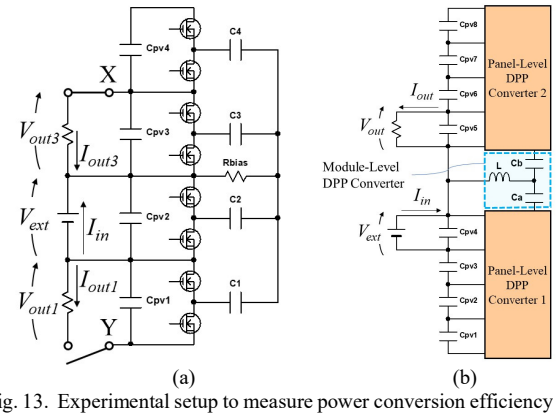

Fig. 13. Experimental setup to measure power conversion efficiency and output characteristics of (a) panel-level DPP converter and (b) module-level DPP converter.

system for two modules, each comprising four panels, was built, as shown in Fig. 12. Components used for the prototype are listed in Table IV. Panel-level DPP converters, which contained C_a or C_b for the module-level DPP converter, were separately built and subsequently connected in series using copper plates. The prototype was operated at 100 kHz with 50% fixed duty cycle.

B. Efficiency and Output Characteristics of Panel- and Module-Level DPP Converters

The power conversion efficiency and output characteristics of the panel-level DPP converter alone were measured using the experimental setup shown in Fig. 13(a). All PV panels were removed, and an external voltage source V_{ext} of 36 V was connected to C_{pv2}. A variable resistor was connected to C_{pv3} or C_{pv1} through the tap X or Y so as to emulate the power transfer between PV_2 and PV_3 or PV_1.

Figure 14(a) shows the measured efficiencies and output characteristics of the panel-level DPP converter. The output voltage (V_{out1} and V_{out3}) monotonically decreased as the output current (I_{out1} and I_{out3}) increased. From the slopes of the measured characteristics of V_{out1} and V_{out3}, the output resistances ($R_{eq.out1}$ and $R_{eq.out3}$) were determined to be 1.16 and 0.81 Ω, respectively. According to the dc equivalent circuit shown in Fig. 10, $R_{eq.out1} = R_{eq.1} + R_{eq.2}$ and $R_{eq.out2} = R_{eq.2} + R_{eq.3}$ can be assumed. Given $R_{eq.2} = R_{eq.3}$ as both C_2 and C_3 are biased to 18 V, the results in Fig. 14(a) yields $R_{eq.1}$ = 0.75 Ω and $R_{eq.2}$ = 0.41 Ω. These experimentally-determined values agreed satisfactorily with the theoretical ones in Table II, verifying the derived dc equivalent circuit in Section V. The measured efficiencies were higher than 92.5% in the region of the output current greater than 0.5 A.

The experimental setup to measure characteristics of the module-level DPP converter is illustrated in Fig. 13(b). An external voltage source $V_{ext.m}$ of 36 V was tied to C_{pv4}, and a variable resistor was connected in parallel with C_{pv5} so as to emulate the case that the power is transferred from Module 1 to Module 2.

The experimental results for the module-level DPP converter are shown in Fig. 14(b). Similar to the panel-level DPP converter, the output voltage linearly declined with the output

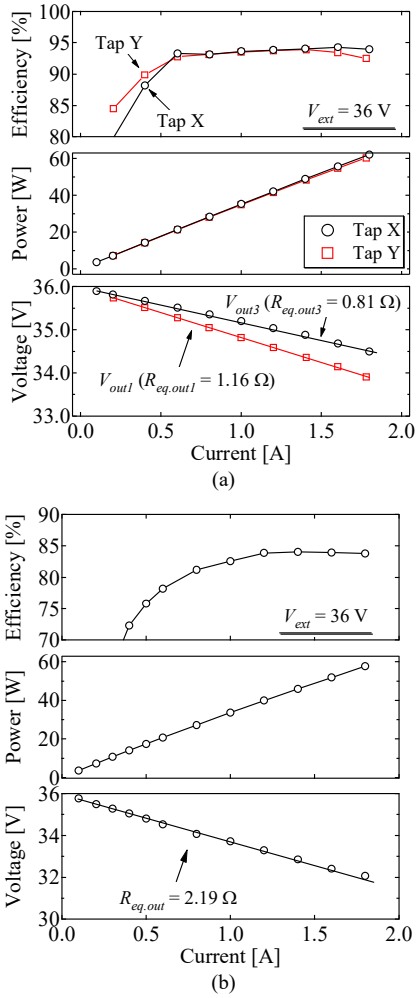

Fig. 14. Measured power conversion efficiency and output characteristics of (a) panel-level DPP converter and (b) module-level DPP converter.

current, and the output resistance $R_{eq.out}$ was determined to be 2.19 Ω from the slope of the measured characteristic. The value of $R_{eq.out}$ theoretically corresponds to $R_{eq.4} + R_{eq.a} + R_{eq.b} + R_{eq.5}$, according to the dc equivalent circuit in Fig. 10. The determined value of $R_{eq.out}$ matched well with the theoretical value of 2.34 Ω (= 0.69 + 0.48 + 0.48 + 0.69 + Ω, see Table II).

C. Laboratory Testing Using Solar Array Simulators

The characteristic mismatch condition due to partial shading was emulated using solar array simulators (Keysight Technologies, E4361A). Individual panel characteristics are shown in Fig. 15(a)—the characteristic of PV_8 was emulated using a constant-current–constant-voltage source with series and parallel resistors due to a lack of solar array simulators in our laboratory. The total power of eight panels in this condition was 1290 W.

Measured string characteristics with/without the prototype are compared in Fig. 15(b). Similar to the simulation results shown in Fig. 11(b), the string characteristic without the modular DPP system (i.e., with bypass diodes) exhibited local MPPs, and its maximum power at the global MPP was 1050 W.

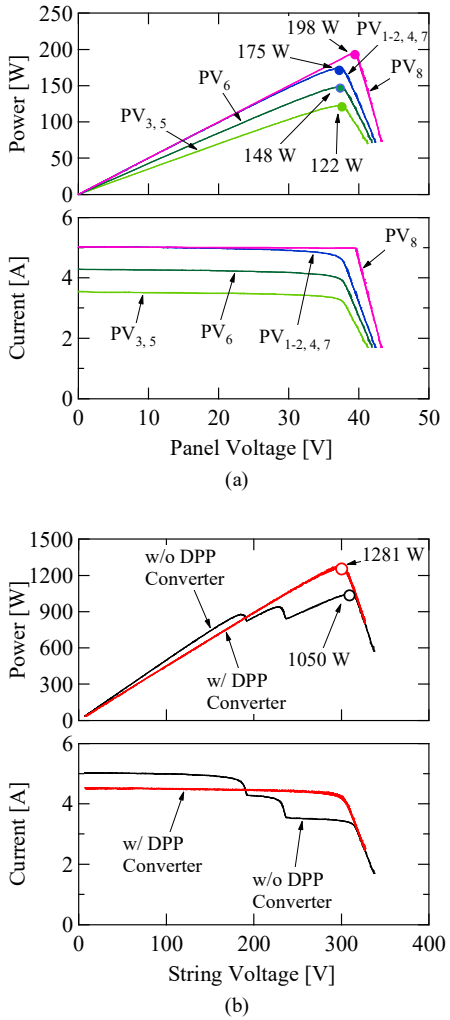

Fig. 15. Experimental results: (a) individual panel characteristics, (b) String characteristics with/without modular DPP system.

Meanwhile, the modular DPP system successfully eliminated the local MPPs, and the extractable maximum power increased to as high as 1281 W at 288 V, corresponding to 22% improvement in power yield. 99.3 % of the theoretical string power (1281/1290 W) could be extracted with the modular DPP system. The measured overall efficiency of 99.3% was higher than the power conversion efficiency of the proposed DPP converter alone (see Fig. 14). This is because the DPP converter literally processed only the differential power between shaded and unshaded panels while most of the string power is directly delivered to the load. Similar experimental results have been reported in the past works; the DPP converters with the power conversion efficiency of 90% achieved overall efficiencies of 96.3% and 91.6% in [13] and [20], respectively.

Measured individual panel voltages when the string operated at the MPP with the DPP system are shown in Table V. The measured voltage difference ΔV_{max} in Module 1 was as low as 0.7 V. Meanwhile, ΔV_{max} in Module 2 was 1.34 V and was considerably larger than that in the simulation analysis probably due to the noticeably mismatched characteristic of PV_8. Despite the mismatched PV_8 characteristic, all the panel and module voltages were adequately unified, demonstrating the voltage equalization performance of the proposed DPP system.

TABLE V
INDIVIDUAL PANEL VOLTAGES WHEN STRING OPERATED AT MPP IN EXPERIMENT

Panel	Voltage
PV_1	37.2
PV_2	37.0
PV_3	36.5
PV_4	37.0
PV_5	35.9
PV_6	36.7
PV_7	37.2
PV_8	37.3

TABLE VI
MEASURED CAPACITOR VOLTAGES OF PROPOSED EQUALIZER WHEN STRING OPERATED AT MPP

Capacitor	Voltage
C_1	57.1 V
C_2	19.2 V
C_3	18.3 V
C_4	55.9 V
C_5	56.2 V
C_6	18.8 V
C_7	18.0 V
C_8	54.5 V
C_a	75.1 V
C_b	74.3 V

Measured capacitor voltages when the string operated at its MPP are shown in Table VI. The observed tendency is very similar to that shown in Table I. Voltages of C_a and C_b were nearly identical, verifying the operation of the switchless DPP converter.

Transient response characteristics were measured emulating sudden irradiance change. Individual panel characteristics in Fig. 15(a) were used as a baseline condition while the short-circuit current of PV_6 was changed between 4.25 A and 5.0 A to emulate sudden irradiance changes. The string voltage was fixed to be 288 V, which corresponded to the MPP voltage in this condition. Recorded transient characteristics are shown in Fig. 16. The panel and module voltages slightly changed because the current flow distribution in the DPP converter also changed in response to the step change in the short-circuit current of PV_6. The measured output power responded within 2 seconds in both cases. These results suggested that the proposed DPP converter could sufficiently unify all panel voltages as well as module voltages even under sudden irradiance changes.

D. Field Testing

The field testing using eight 60-cell monocrystalline PV panels was performed in Hitachi, Japan, on December 14th, 2018 at 11:00. The irradiance level was measured using a pyranometer (ES-602, EKO). The experimental setup of the field testing is shown in Fig. 17. PV_8 in Module 2 was intentionally partially-shaded with a plastic bag.

Before sweeping string characteristics, individual panel characteristics in Modules 1 and 2 were measured, as shown in

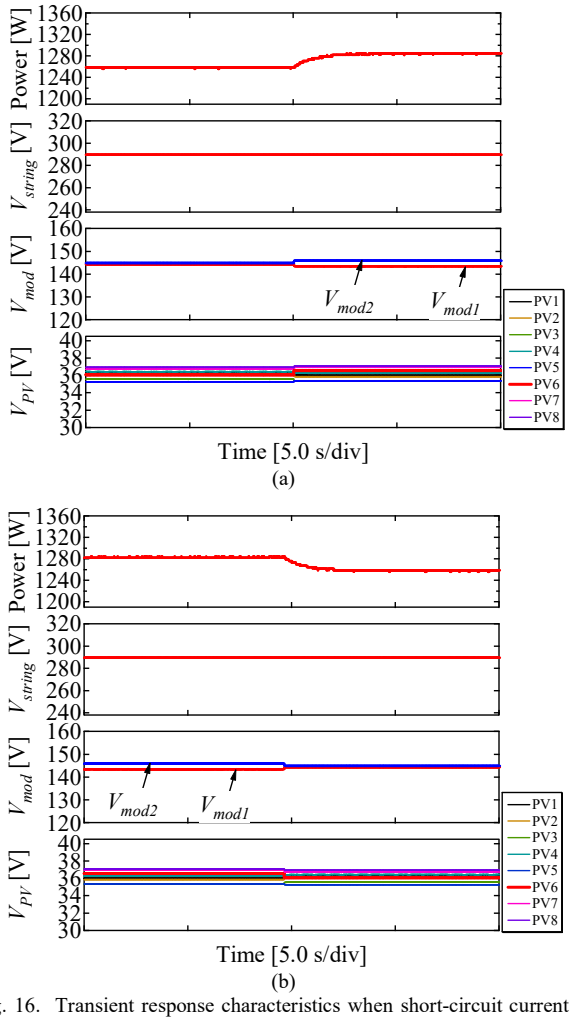

Fig. 16. Transient response characteristics when short-circuit current of PV_6 is (a) step-increased and (b) step-decreased.

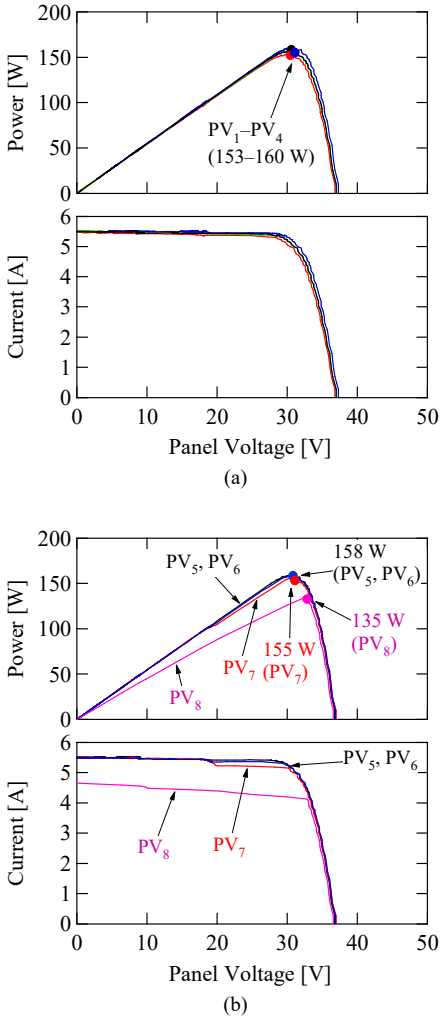

Fig. 18. Individual panel characteristics in (a) Module 1 and (b) Module 2 in field testing.

Figs. 18(a) and (b), respectively. The irradiance level at the moment of the characteristic sweep was measured to be 527 W/m^2. Characteristics in Module 1 were nearly uniform, and maximum powers were in the range of 153–160 W [see Fig. 18(a)]. In Module 2, on the other hand, measured characteristics were mismatched due to the plastic bag on PV_8, and the maximum power of PV_8 was 135 W [see Fig. 18(b)]. The sum of maximum powers of PV_1–PV_8 was 1234 W under this partial shading condition.

The measured string characteristics with/without the modular DPP system are shown in Fig. 19. The measured string characteristic without the DPP converter was somewhat elusive, but it obviously exhibited a local MPP. The extractable power at the global MPP was 1099 W. With the proposed modular DPP system, the local MPP disappeared, and maximum power increased to as high as 1223 W. This result was equivalent to 11.1% improvement in power yield, and 99.1% (= 1223 W/1234 W) of the string power was extractable, hence demonstrating the efficacy of the proposed modular DPP system in the field testing.

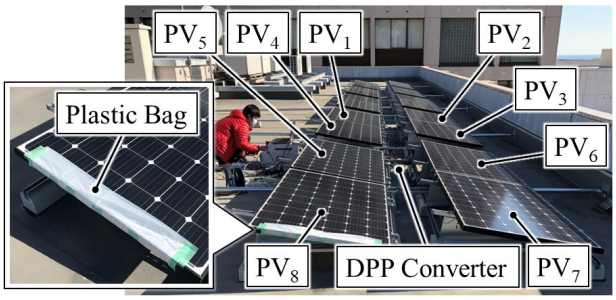

Fig. 17. Experimental setup for field testing.

IX. Conclusions

The SCC-based modular DPP architecture for PV strings has been proposed in this paper. In the proposed modular system, modules containing series-connected PV panels with a panel-level DPP converter are connected through a switchless module-level DPP converter. The number of panels in each module is fixed and unchanged, while the number of modules can be arbitrarily extended by adding modules with module-level DPP converter, achieving good modularity. Voltage

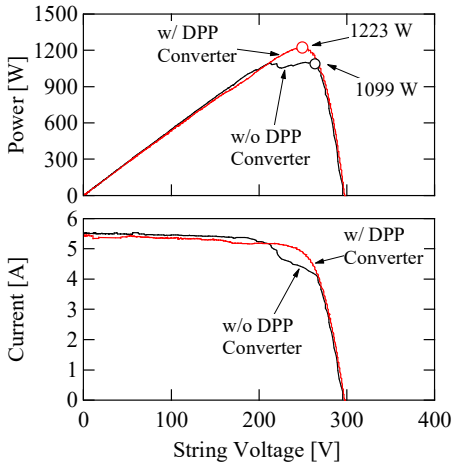

Fig. 19. Measured string characteristics with/without modular DPP system in field testing.

stresses of the capacitors in the proposed modular system can be reduced lower than half the module voltage, allowing all-MLCC topology and miniaturized circuit design.

The prototype for the PV string consisting of two modules, each comprising four panels, was built, and the laboratory and field testing was performed emulating partial shading conditions. With the support of the proposed modular DPP system, local MPPs in the measured string characteristics successfully disappeared, and the power yield dramatically increased, demonstrating the efficacy of the proposed modular DPP system.

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