Single-Switch Single-Transformer Cell Voltage Equalizer Based on Forward-Flyback Resonant Inverter and Voltage Multiplier for Series-Connected Energy Storage Cells

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***Abstract*— Cell voltage equalization is inevitable to ensure years of safe operation of series-connected energy storage cells, such as lithium-ion batteries and supercapacitors (SCs). Although various kinds of cell voltage equalizers have been proposed, most equalizer topologies require multiple switches and/or a multi-winding transformer, resulting in complex circuitry and poor modularity. In this paper, a single-switch single-transformer equalizer using a forward-flyback resonant inverter (FFRI) with voltage multiplier is proposed. The required switch count of the proposed equalizer is the minimum without impairing modularity due to the single-switch circuitry with no need of a multi-winding transformer. An experimental equalization test performed for eight SCs connected in series successfully demonstrated the equalization performance of the proposed equalizer. The FFRI can be extended as "resonant input cell", and by combining one of resonant input cells and a voltage multiplier, a single-switch resonant equalization charger that is basically a charger with an equalization function is also derived. An experimental charging test using the resonant equalization charger was also performed and its equalization-charging performance was demonstrated.**

***Index Terms*— Battery, equalizer, forward-flyback inverter, supercapacitor, voltage imbalance, voltage multiplier.**

I. Introduction

The applications of energy storage cells, such as lithium-ion batteries and supercapacitors (SCs), have been increasingly expanding from personal electronic devices, such as cellphones and laptop computers, to large-scale energy storage systems, including vehicular applications and grid-connected renewable energy systems using photovoltaic panels and wind power generators. Lithium-ion batteries are now regarded as the most promising energy storage device not only for terrestrial use but also aerospace applications, including spacecraft and the latest jetliners, where reliability is of primary importance since even a single failure may be fatal and cause irretrievable malfunctions. As is well known, precise battery management is also imperative for lithium-ion batteries to preclude overcharging and over-discharging and ensure years of safe operation. Failure to do so may result in premature irreversible deterioration or, in the worst case, explosion as has frequently been reported. SCs have equivalent issues and restrictions, although the requirement of safety and precision for SCs is somewhat mitigated due to their safer characteristics.

Cell voltage equalization for energy storage modules/systems comprising multiple cells connected in series is an inevitable requirement to ensure years of safe operation. The voltages of series-connected cells gradually become imbalanced due to the nonuniformity of individual cells in terms of capacity, internal impedance, and self-discharge rate. Some cells in a voltage-imbalanced battery pack may be overcharged/over-discharged even though a pack voltage is within a safety boundary. The issue in terms of voltage imbalance can be mitigated by cell screening; individual cells are screened to minimize any nonuniformity in series-connected cells [1]. However, the cell screening process is lengthy and costly since individual cell characteristics need to be measured and compared to select proper cells. Furthermore, the nonuniform self-discharge rate attributable to the temperature gradient in a module/system cannot be obviated by cell screening. Accordingly, cell voltage equalizers are considered necessary and used in most applications.

Equalization techniques can be roughly categorized into two: passive and active equalizations [2], [3]. Passive equalization techniques rely on resistors or Zener diodes that dissipate stored energy in cells to equalize cell voltages, reducing energy efficiency. With active equalization techniques, conversely, stored energy in cells with higher voltage is transferred to cells with lower voltage so that all cell voltages become uniform by redistributing stored energy.

Various active equalization techniques have come in handy, but most conventional active equalization topologies have issues in terms of complexity (or reliability), modularity, or size. The number of switches necessary to compose equalizers is considered a good indicator of circuit complexity because each switch requires several ancillary components, including a gate driver IC, opto-coupler, and passive components. Most common approaches are to use multiple dc-dc converters [4], [5], bidirectional buck-boost converters [6]–[10], and switched

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capacitor converter [11]–[19], to transfer energy/charge between two adjacent cells for equalization. However, the number of switches required in these approaches is proportional to the number of cells connected in series; hence the circuitry tends to become more and more complex with increasing series connections. Equalizers using selection switches can significantly reduce the number of passive components [20]–[26], and are considered suitable for applications requiring numerous cells in series, such as electric vehicles. However, the required number of switches still increases with the number of series connections. Furthermore, an intelligent management system using battery management ICs is imperative to determine target cells, namely those with the highest/lowest voltage, to execute equalization. Equalizers using a multi-winding transformer may comprise one or two switches [27]–[30], dramatically reducing the circuit complexity. However, the strict parameter matching requirement for multiple secondary windings of a multi-winding transformer is considered to hinder efforts to achieve good modularity [2], [3]. A single-switch equalizer using multi-stacked buck-boost converters [31] would be the best topology to simplify the circuitry, but the inductor count is proportional to the number of cells, likely increasing the equalizer's size.

Equalizers using an inverter and voltage multiplier have been proposed to reduce the switch count; two-switch configurations with no need of a multi-winding transformer are feasible [32], [33]. A half-bridge or resonant inverter is used to produce the ac voltage/current wave required to drive the voltage multiplier. Although these equalizers are very simple, two switches are still necessary, as well as a boot-strap gate driver for a high-side switch. Accordingly, reducing the switch count to one and eliminating the high-side switch would further simplify the equalizers' circuitry. A single-switch equalization charger combining a charger and equalizer to simplify an energy storage system as a whole has also been proposed for small power applications [34]. From a circuit simplicity perspective, the single-switch equalization charger would be the most attractive topology, but tends to be linked to a relatively large inrush current, likely posing issues on current stresses of devices and EMI.

A forward-flyback inverter (FFI) [35], [36], a single-switch inverter, would be an attractive candidate for driving the voltage multiplier and further simplifying the circuitry of equalizers. To achieve flyback operation, a gapped core is usually necessary for a transformer to store sufficient magnetizing energy, but the leakage inductance of such gapped-transformers also tends to be considerable. Meanwhile, a relatively large current flows in the transformer because both magnetizing and forward current flow while a switch is on, which is likely to result in an increased loss in a snubber circuit — the snubber loss is generally proportional to leakage inductance and the square of the current at turn-off transition [37].

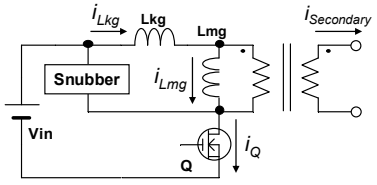
A single-switch voltage equalizer using a forward-flyback resonant inverter (FFRI) with voltage multiplier is proposed in this paper. The required switch count of the proposed equalizer can be minimized without impairing modularity due to the single-switch circuitry with no need of a multi-winding transformer. The resonant operation can considerably reduce the turn-off switching loss as well as snubber loss compared with an FFI. Section II describes the individual FFI/FFRI and voltage multiplier circuits, from which the proposed single-switch voltage equalizer is derived. The FFRI and FFI operations are qualitatively compared, and detailed operation analyses for the voltage multiplier and FFRI are separately performed and respective dc equivalent circuits are mathematically obtained in Section III. Simulation analyses for both the original and derived dc equivalent circuits are performed for verification in Section IV. The experimental fundamental performances of equalizers using the FFRI and FFI are compared in Section V, and the result of the equalization performed for eight SCs connected in series is presented. In Section IV, feasible extended single-switch topologies for resonant equalization chargers are also discussed, and some experimental results for a resonant equalization charger are shown.

II. Single-Switch Voltage Equalizer Using Forward-Flyback Resonant Inverter with Voltage Multiplier

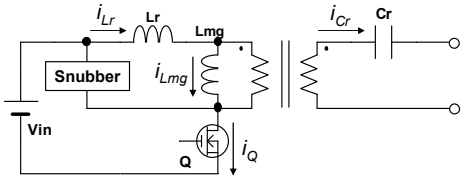
A. Forward-Flyback Inverters and Voltage Multiplier

From the combination of an FFI/FFRI and a voltage multiplier, as shown in Figs. 1 and 2, respectively, the proposed single-switch voltage equalizer can be derived. When the switch Q is on, power is transferred to the secondary side in a forward mode, while the magnetizing inductance of the transformer, L_{mg}, stores magnetizing energy. As the switch is turned off, the stored energy in L_{mg} is discharged and transferred to the secondary side. Hence, an ac voltage/current is generated at the secondary side. The detailed operation will be discussed in Section III.

The voltage multiplier shown in Fig. 2 is a representative circuit for four cells connected in series. This voltage multiplier consists of energy transfer capacitors C_1–C_4, smoothing capacitors C_{out1}–C_{out4}, and diodes D_1–D_8, meaning there is no active switch or magnetic component. As an ac voltage/current wave is applied to the input, the



(a) Forward-flyback inverter



(b) Forward-flyback resonant inverter.

Fig. 1. (a) Forward-flyback inverter (FFI) and (b) forward-flyback resonant inverter (FFRI).

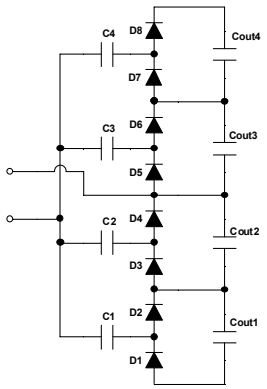


Fig. 2. Voltage multiplier for four cells connected in series.

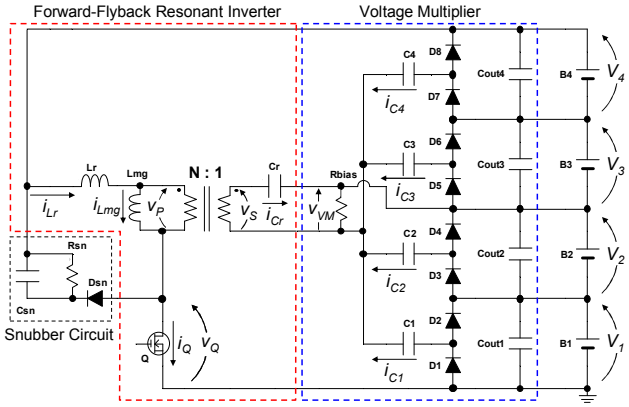


Fig. 3. Single-switch voltage equalizer using a forward-flyback resonant inverter with voltage multiplier for four cells connected in series.

voltages of C_{out1}–C_{out4} automatically become uniform. The theoretical analysis for the voltage multiplier driven by the FFRI will be performed in Section III-C.

B. Proposed Single-Switch Voltage Equalizer

By combining the FFI/FFRI and voltage multiplier shown in Figs. 1 and 2, respectively, the proposed single-switch voltage equalizer can be derived. Figure 3 illustrates the topology using the FFRI with the voltage multiplier for four cells B_1–B_4 connected in series. Although an RCD snubber is used in Fig. 3, any snubber circuits, including nondissipative snubber circuits [38], [39], can be used. R_{bias} in the voltage multiplier is a high-resistance resistor with which the voltage of C_r, V_{Cr}, is biased to zero under a steady-state condition. The series connection of B_1–B_4 powers the FFRI, whereupon the supplied power is transferred to the voltage multiplier as ac voltage/current. The voltage multiplier operates so that the power is preferentially distributed to a cell with the lowest voltage (i.e. the least charged cell). This means the energy of the series-connected cells is circulated through the proposed voltage equalizer, and all the cell voltages are automatically unified in the course of the energy circulation. A detailed operational analysis will be performed in the next section.

Similar to conventional flyback converters operating in discontinuous conduction mode (DCM), current in the proposed equalizer can be limited under desired current levels, even without feedback control, by properly designing the equalizer and determining operation conditions (Section III-D). This allows the feedback control loop to be eliminated, further simplifying the circuitry.

The prominent feature of the proposed equalizer is the single-switch circuitry. Although previously proposed equalizers using voltage multipliers [32], [33] are also simple, the switch count is two, double that of the proposed equalizer, and a boot-strap gate driver for the high-side switch is required. In addition to the single-switch circuitry, the single-magnetic topology is feasible if the leakage inductance of the transformer is utilized as a resonant inductor L_r for the FFRI; in the FFI, L_{kg} and L_{mg} in Fig. 1(a) are, of course, in a single transformer. Furthermore, the transformer in the proposed equalizer is a normal one with two windings (i.e. primary and secondary), not a multi-winding transformer that impairs the design and modularity [2], [3]. Therefore, the proposed equalizer is considered the simplest ever equalization topology retaining unimpaired modularity.

On the other hand, drawbacks of the proposed voltage equalizer include unfeasible state of charge (SOC) equalization and efficiency penalty due to collective diode losses in the voltage multiplier. Some conventional equalizers, such as [5], [24], [25], can equalize SOCs of cells by individually controlling multiple switches, although control algorithms and management system tend to be complex. On the other hand, the SOC equalization is unfeasible with the proposed voltage equalizer because the single-switch topology cannot individually control SOCs; it is the cell voltages that are equalized by the proposed equalizer, as will be discussed in Section III-C.

Efficiency performance of the proposed voltage equalizer might be inferior to conventional ones based on synchronous converters because of the collective losses of each diode forward voltage drop that takes significant portion of the relatively low output voltages (i.e., cell voltages), which are usually lower than 3.0 and 4.2 V for SCs and lithium-ion cells, respectively; the conventional equalizer using a synchronous converter with selection switches, for example, achieves a peak efficiency of 90%, whereas the measured peak efficiency of the 6-W prototype is approximately 80%, as will be shown in Section V-B. However, the inferior efficiency performance is considered acceptable in many applications because required power capability for equalizers is rather smaller than rated power of energy storage modules. In general, required power capability for equalizers is determined so that voltage imbalance originating from mismatch in individual cell characteristics can be eliminated or precluded. As long as energy storage modules are properly designed and manufactured, characteristic mismatch is not significant, and hence, low power equalizers are enough to eliminate voltage imbalance. For example, an equalization current that is 100 times smaller than a charging current is considered sufficient during float charging [12], [40], although the optimum equalization current rate would be dependent on applications.

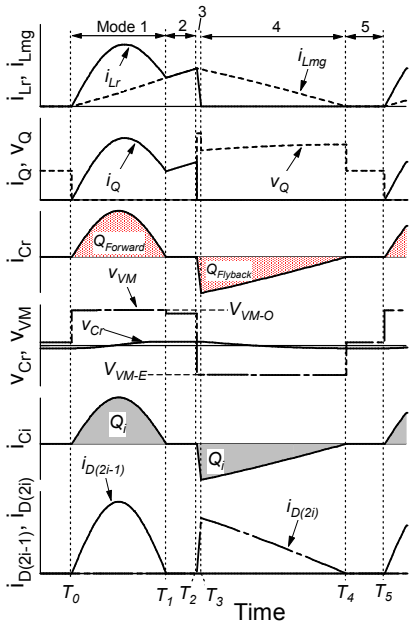


Fig. 4. Key operation waveforms of the equalizer using FFRI.

III. Operating Analysis

The operation of the overall equalizer is first briefly explained in this section, followed by separate detailed analyses for the voltage multiplier and FFRI. DC equivalent circuits for both the voltage multiplier and FFRI are separately derived, whereupon the dc equivalent circuit for the whole equalizer is obtained by combination.

A. Operation Waveforms and Current Flows

In this subsection, the operation and current flow paths of the proposed equalizer using the FFRI are explained. However, the operation of that using the FFI can be understood similarly and is compared with that using the FFRI in the next subsection. To simplify the analysis, the following premises are introduced: 1) the inductance of L_r, L_r, is much smaller than that of L_{mg}, L_{mg}, and hence, the current of L_{mg}, i_{Lmg}, linearly changes, 2) the total capacitance of C_i ($i = 1…4$) viewed from C_r is sufficiently larger than C_r, and C_i does not influence the resonant operation, and 3) the average voltage of C_r is zero thanks to R_{bias}. The key operation waveforms and current flow directions are shown in Figs. 4 and 5, respectively. For simplicity, the snubber capacitor is equivalently illustrated as a voltage source of V_{sn}, and the bias resistor R_{bias} and smoothing capacitors C_{out1}–C_{out4} are not illustrated in Fig. 5.

In DCM operation, the current of Q, i_Q, at the beginning of the first mode, Mode 1, is zero, achieving zero-current switching (ZCS). L_r and C_r resonate and i_{Lr} changes sinusoidally, while i_{Lmg} linearly increases. At the same time, the odd-numbered diodes, $D_{(2i-1)}$ (i = 1…4), are conducting in the voltage multiplier. Mode 1 lasts until i_{Lr} and i_{Lmg} become the same. In the next mode, Mode 2, i_{Lmg} continues to linearly increase, while no current flows on the secondary side or voltage multiplier.

By turning off Q, Mode 3 begins, the energy stored in L_r is buffered in the snubber circuit, and i_{Lr} starts falling linearly. The discharge of the stored energy in L_{mg} to the secondary side starts, and the even-numbered diodes, $D_{(2i)}$, start conducting. As i_{Lr} declines to zero, Mode 4 begins. Except for the current path in the snubber circuit, the current flow directions in Modes 3 and 4 are identical; current in the voltage multiplier fall linearly as stored energy in L_{mg} is released to the secondary side. After i_{Lmg} declines to zero and the stored energy in L_{mg} is fully discharged, the operation shifts to Mode 5, in which no current flows.

Energy is transferred to the secondary side in forward mode

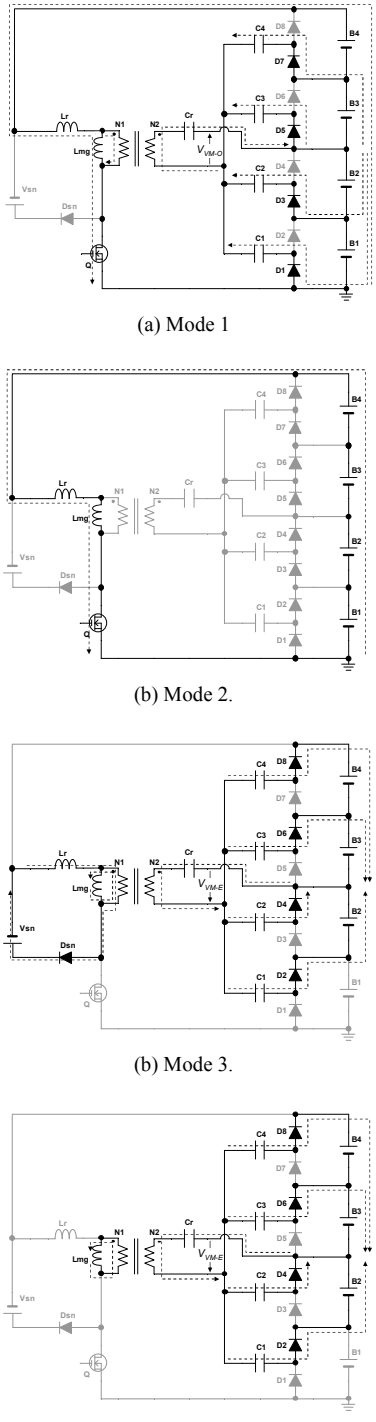
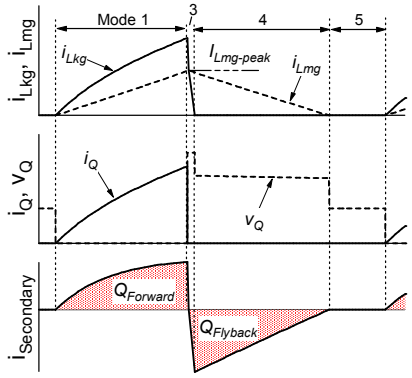


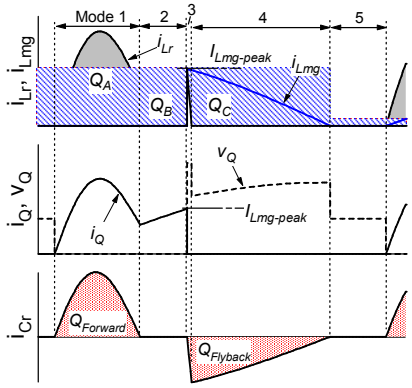
Fig. 5. Current flow directions.

in Mode 1. Meanwhile, the equalizer also operates in flyback mode since the energy stored in L_{mg} during Modes 1 and 2 is transferred to the secondary side during Modes 3 and 4.

As can be seen in Fig. 5, currents flowing through outer cells (B_1 and B_4) are superimposed on inner cells (B_2 and B_3) because the output of the FFRI is connected to the junction of B_2 and B_3; the current from C_3 in Mode 3, for example, flows toward B_3 only, whereas that from C_4 flows through both B_3 and B_4. Practically, these currents are buffered by a smoothing capacitor $C_{out\text{-}i}$, which is connected to each cell in parallel (see Fig. 3). Regardless of the number of series-connected cells, the current of $C_{out\text{-}i}$ never exceed that of C_r, i_{Cr}, because all the currents in the voltage multiplier come from/back to C_r, as shown in Fig. 5. Therefore, $C_{out\text{-}i}$ should be designed considering i_{Cr} that will be expressed by (10) and (18) in Section III-D. On the other hand, the larger the number of series-connected cells, the larger will be the number of smoothing capacitors that are contained in the current paths of i_{Cr}, resulting in increased Joule loss. This would limit the number of cells that the proposed equalizer can be applied — empirically, eight to twelve cells are acceptable to achieve a peak efficiency of 70–80%, as experimentally demonstrated in Section V for eight cells connected in series. For energy storage systems consisting of a large number of cells, the modularized structure design [17], which introduces intra- and outer-module equalizers to reduce the number of cells supported by a single equalizer, would be effective.



(a) FFI.



(b) FFRI.

Fig. 6. Comparison for key operation waveforms between (a) FFI and (b) FFRI.

B. Comparison between Forward-Flyback Resonant and Nonresonant Inverters

The key operation waveforms of an FFI and FFRI are shown and compared in Fig. 6. Both inverters achieve ZCS at turn-on. The current flow paths in the FFI are very similar to those in the FFRI explained in the previous subsection, except for Mode 2, in which the current on the secondary side, i_{Cr}, is zero, as shown in Figs. 4 and 6(b). The switch current, i_Q, in Mode 2 in the FFRI is identical to i_{Lmg}, and its value at the moment of turn-off is $I_{Lmg\text{-}peak}$. In the FFI, conversely, the current on the secondary side, $i_{Secondary}$, increases according to a typical transient current response expressed as, $i_{Secondary} \propto 1-\exp(-t/\tau)$, where τ is the time constant expressed as $\tau = N^2L_{kg}/R$ (R is the resistive component in the current path), while the waveform of i_{Lmg} is identical to that of the FFRI. i_Q as well as i_{Lkg} consistently increase while Q is on, as shown in Fig. 6(a), while the value of i_Q at turn-off exceeds $I_{Lmg\text{-}peak}$, causing larger turn-off switching loss and snubber loss than those in the FFRI. The FFRI is therefore considered advantageous over the FFI from the perspective of reducing these losses. Because superior performance is expected in the FFRI, a detailed analysis is performed only for the FFRI in the following sections.

C. Analysis for the Voltage Multiplier

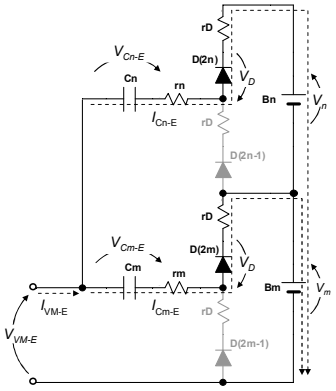
The circuitry of the voltage multiplier in the proposed equalizer is identical to that in conventional voltage equalizers. However, the operation of the voltage multiplier depends on the type of inverter used to drive the voltage multiplier. From a technical perspective, the operation of voltage multipliers driven by a half-bridge or resonant inverter in previous works are symmetrical [32], [33], whereas that driven by the FFRI in the proposed equalizer is asymmetric. The operational analysis for the voltage multiplier in this subsection is somewhat similar to that in the previous work [33]; the voltage multiplier is assumed to operate in two modes, Modes E and O, in which even- and odd-numbered diodes are on, respectively. To simplify the analysis, the impedances of smoothing capacitors are assumed to be minimal, and a voltage multiplier for two cells, B_m and B_n, shown in Fig. 7, is considered.

The average current flowing through each capacitor C_i (i = m or n) over Modes E and M, $I_{Ci\text{-}E}$ and $I_{Ci\text{-}O}$, can be expressed as

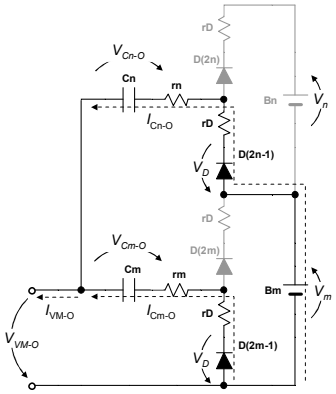
$$\begin{cases} I_{Ci-E} = \dfrac{Q_i}{0.5T_r} = 2f_rQ_i \\ I_{Ci-O} = \dfrac{Q_i}{D'T_S} = \dfrac{f_SQ_i}{D'} \end{cases}, \tag{1}$$

where Q_i is the charge delivered through C_i designated in Fig. 4, T_r and T_S are the resonant and switching periods, f_r and f_S are the resonant and switching frequency, and D' is the duty cycle of Mode O, which will be expressed by (19) in the next subsection. The input voltages of the voltage multiplier during Modes E and O, $V_{VM\text{-}E}$ and $V_{VM\text{-}O}$, are

$$\begin{aligned} V_{VM-E} &= V_m - V_{Cm-E} + V_D + I_{Cm-E}(r_m + r_D) \\ &= V_m + V_n - V_{Cn-E} + V_D + I_{Cn-E}(r_n + r_D), \end{aligned} \tag{2}$$



(a) Mode E.



(b) Mode O.

Fig. 7. Operation modes of voltage multiplier in (a) Mode E and (b) Mode O.

$$\begin{aligned} V_{VM-O} &= V_{Cm-O} + V_D + I_{Cm-O}\left(r_m + r_D\right) \\ &= -V_m + V_{Cn-O} + V_D + I_{Cn-O}\left(r_n + r_D\right), \end{aligned} \tag{3}$$

where $V_{Ci\text{-}E}$ and $V_{Ci\text{-}O}$ ($i = m$ or n) are the voltage of C_i during Modes E and O, V_D is the diode forward voltage, r_i and r_D are the ESR of C_i and slope resistance of diodes, respectively. From (2) and (3), the voltage variation of C_i in a single switching cycle, ΔV_{Ci}, is yielded as

$$\begin{aligned} \Delta V_{Ci} &= V_{Ci-O} - V_{Ci-E} \\ &= \left(V_{VM-O} + V_{VM-E}\right) - V_i - 2V_D - \left(I_{Ci-E} + I_{Ci-O}\right)\left(r_i + r_D\right). \end{aligned} \tag{4}$$

By introducing the average current flowing through C_i over half the switching period, $I_{Ci} = Q_i f_S = C_i \Delta V_{Ci} f_S$, the substitution of (1) into (4) produces

$$V_{VM-O} + V_{VM-E} = V_i + 2V_D + I_{Ci} R_{eq-i}, \tag{5}$$

where $R_{eq\text{-}i}$ is the equivalent resistance expressed as

$$R_{eq-i} = \frac{1}{C_i f_S} + \left(2\frac{f_r}{f_S} + \frac{1}{D'}\right)\left(r_i + r_D\right). \tag{6}$$

The sum of I_{Ci} is defined as I_{VM},

$$I_{VM} = \sum_i^n I_{Ci}, \tag{7}$$

where n is the number of cells connected in series.

Equations (5)–(7) derive a dc equivalent circuit of the voltage multiplier, as shown in Fig. 8, which resembles those in conventional equalizers. Except for the value of derived $R_{eq\text{-}i}$ in (6), the fundamentals, including equalization mechanism and concerns about parameter mismatch discussed in detail in [33], are similar to those of voltage multipliers in conventional equalizers.

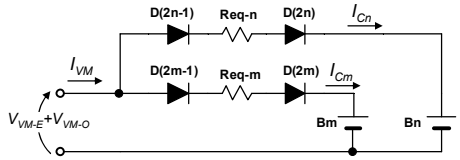


Fig. 8. DC equivalent circuit of voltage multiplier.

The derived dc equivalent circuit implies that any parameter mismatch in $R_{eq\text{-}i}$ and V_D would lead to a residual voltage imbalance because all cells are connected to the common terminal through respective $R_{eq\text{-}i}$ and two diodes. A residual voltage imbalance due to a mismatch in V_D cannot be compensated, because V_D is basically independent of operation conditions, such as switching frequency, duty cycle, current, etc. Conversely, a residual voltage imbalance due to mismatch in $R_{eq\text{-}i}$, may be kept negligible by selecting proper components and properly determining operation conditions. To limit the residual voltage imbalance within an acceptable range, the residual voltage imbalance must be estimated considering the largest possible parameter mismatch in $R_{eq\text{-}i}$.

By assuming that B_i is a pure capacitor with a capacitance of C_{Bi}, the current flowing toward B_i is expressed as $I_{Ci} = C_{Bi}(dV_i/dt)$. Under a steady-state condition whereby all of V_i are balanced, dV_i/dt is uniform for all cells. Therefore, I_{VM} is uniformly distributed to all of B_i as long as C_{Bi} is uniform (see I_{C1}–I_{C4} 600 ms after the beginning of simulation analyses shown in Fig. 12), and its value is $I_{Ci} = I_{VM}/n$. By defining the maximum and minimum $R_{eq\text{-}i}$ in a voltage multiplier as $R_{eq\text{-}max}$ and $R_{eq\text{-}min}$, respectively, the residual voltage imbalance due to mismatch in $R_{eq\text{-}i}$, $V_{Residual}$, can be estimated as

$$V_{\mathrm{Re}sidual} = \frac{I_{VM}}{n}\left(R_{eq-\max} - R_{eq-\min}\right). \tag{8}$$

D. Operation Analysis for Forward-Flyback Resonant Inverter

In this subsection, the FFRI is analyzed based on equivalent circuits shown in Fig. 9. The average voltage of the transformer secondary winding is zero, and due to the bias resistor R_{bias} connected to C_r (see Fig. 4), the average voltage of C_r, V_{Cr}, is also zero, as mentioned in Section III-A. For simplicity, it is assumed that i_{Lmg} varies linearly in all operation modes and the voltage variation of C_r is small enough compared with $V_{VM\text{-}E}$ and $V_{VM\text{-}O}$.

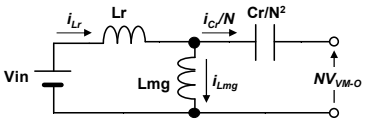
i) Mode 1 ($T_0 < t < T_1$):

The current of L_{mg}, i_{Lmg}, linearly increases from zero, expressed as

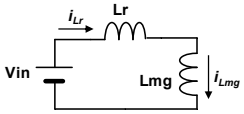
$$i_{Lmg}(t) = \frac{V_{in}}{L_r + L_{mg}}\left(t - T_0\right). \tag{9}$$

Since V_{Cr} can be regarded as zero, the current of C_r/N^2, $i_{Cr}(t)/N$, is given by

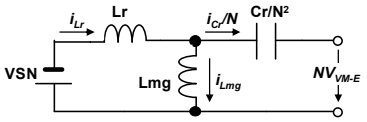
$$\frac{i_{Cr}(t)}{N} = \frac{V_{in} - NV_{VM-O}}{|Z_r|}\sin\omega_r\left(t - T_0\right), \tag{10}$$



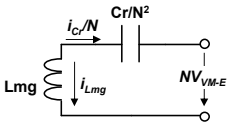
(a) Mode 1



(b) Mode 2.



(b) Mode 3.



(b) Mode 4.

Fig. 9. Equivalent circuits of FFRI during operation in (a) Mode 1, (b) Mode 2, (c) Mode 3, and (d) Mode 4.

where V_{VM-O} is the input voltage of the voltage multiplier while odd-numbered diodes are on (see Fig. 5(a)), and Z_r and ω_r are the characteristic impedance and resonant angular frequency, respectively, as given by

$$|Z_r| = N\sqrt{\frac{L_r}{C_r}}, \quad \omega_r = \frac{N}{\sqrt{L_r C_r}}. \tag{11}$$

When $i_{Cr}(t)/N$ becomes zero at $t = T_1$, V_{VM-O} can be approximated as

$$NV_{VM-O} = \frac{V_{in} L_{mg}}{L_r + L_{mg}}. \tag{12}$$

For the next mode, Mode 2, to exist, the following equation must be satisfied:

$$D \geq \frac{f_S}{2 f_r}, \tag{13}$$

where D is the duty cycle of Q.

ii) *Mode 2* ($T_1 < t < T_2$):

i_{Lmg} continues to increase at the same rate as in Mode 1, and its peak value at the end of Mode 2, $I_{Lmg\text{-}peak}$, is

$$I_{Lmg-peak} = \frac{V_{in} D T_S}{L_r + L_{mg}}. \tag{14}$$

iii) *Mode 3* ($T_2 < t < T_3$):

The stored energy in L_r is absorbed in the snubber circuit in Mode 3. The length of Mode 3, T_{SN}, is yielded as

$$T_{SN} = \frac{I_{Lmg-peak} L_r}{V_{SN} - NV_{VM-E}}, \tag{15}$$

where V_{SN} is the voltage of the snubber capacitor equivalently illustrated as a voltage source of V_{SN} in Figs. 5 and 9(c), while V_{VM-E} is the input voltage of the voltage multiplier while even-numbered diodes are on (see Figs. 5(c) and (d)). By defining $k = V_{SN}/NV_{VM-E}$ and substituting (14), (15) can be rewritten as

$$T_{SN} = \frac{L_r}{L_r + L_{mg}} \frac{V_{in} D T_S}{(k-1) NV_{VM-E}}. \tag{16}$$

By neglecting the voltage drop due to $R_{eq\text{-}i}$ in (5) and substituting (12), V_{VM-E} can be simplified to

$$NV_{VM-E} = \frac{N(L_r + L_{mg})(V_i + 2V_D) - V_{in} L_{mg}}{L_r + L_{mg}}. \tag{17}$$

i_{Lmg} linearly decreases as

$$i_{Lmg}(t) = I_{Lmg-peak} - \frac{NV_{VM-E}}{L_{mg}}(t - T_2). \tag{18}$$

iv) *Mode 4* ($T_3 < t < T_4$):

i_{Lmg} continues to decrease at the same rate as in Mode 3, and i_{Lmg} becomes zero at $t = T_4$. From $T_4 - T_2 = D'T_S$, (14), (17), and (18),

$$D' = \frac{DV_{in}}{N(V_i + 2V_D)\dfrac{L_r + L_{mg}}{L_{mg}} - V_{in}}. \tag{19}$$

For the FFRI to operate in DCM, $D' < (1 - D)$ must be ensured. From (19), the critical duty cycle to ensure the DCM operation, $D_{critical}$, can be yielded as

$$D_{critical} < 1 - \frac{L_{mg} V_{in}}{N(L_r + L_{mg})(V_i + 2V_D)}. \tag{20}$$

The areas Q_A–Q_C designated in Fig. 6(b) can be expressed as

$$\begin{cases} Q_A = Q_C = \dfrac{I_{Lmg-peak}(D'T_S - T_{SN})}{2} \\ Q_B = \dfrac{I_{Lmg-peak} D T_S}{2} \end{cases}. \tag{21}$$

Using (14), (20), and (21), the average input current of the FFRI, $I_{in\text{-}ave}$, is yielded as

$$I_{in-ave} = \frac{Q_A + Q_B}{T_S} = \frac{V_{in} D T_S}{2(L_r + L_{mg})}\left\{D + D'\left(1 - \frac{L_r}{(k-1)L_{mg}}\right)\right\}. \tag{22}$$

As expressed by (19), D' depends on V_{in} and V_i, and its variation range can be easily estimated from those of V_{in} and V_i. Therefore, from (19) and (22) with known variation ranges of V_{in} and V_i, $I_{in\text{-}ave}$ can be limited under a desired current level, even without feedback control, by properly determining and designing D, L_r and L_{mg}.

Equation (22) can be rewritten as

$$\begin{aligned} I_{in-ave} = I_{mg} + I_T &= V_{in} \frac{\pi D^2 + \pi D D'\left(1 - \dfrac{L_r}{(k-1)L_{mg}}\right)}{\omega_S (L_r + L_{mg})} \\ &= V_{in} \frac{R_{mg} + R_T}{R_{mg} R_T} \end{aligned}, \tag{23}$$

where ω_S is the angular switching frequency, and I_{mg}, I_T, R_{mg}, and R_T are given by

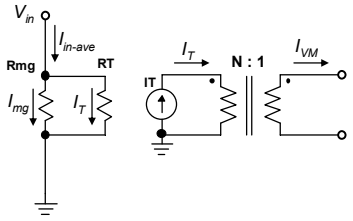


Fig. 10. DC equivalent circuit of FFRI.

$$\begin{cases} I_{mg} = \dfrac{Q_B}{T_S} = V_{in}\dfrac{\pi D^2}{\omega_S\left(L_r + L_{mg}\right)} = \dfrac{V_{in}}{R_{mg}} \\ I_T = \dfrac{Q_A}{T_S} = V_{in}\dfrac{\pi DD'\left(1 - \dfrac{L_r}{(k-1)L_{mg}}\right)}{\omega_S\left(L_r + L_{mg}\right)} = \dfrac{V_{in}}{R_T} \end{cases} . \quad (24)$$

From (23) and (24), a dc equivalent circuit of the FFRI can be derived as shown in Fig. 10. Since it is a dc circuit, the transformer is the ideal one allowing dc components to flow. In the derived dc equivalent circuit, all symbols and components have their own functional meaning. I_{mg}, the current flowing through R_{mg}, corresponds to the average current used to magnetize L_{mg}. Meanwhile, I_T corresponds to the average current transferred to the voltage multiplier through the transformer.

E. Derivation for DC Equivalent Circuit

By combining dc equivalent circuits of the voltage multiplier and FFRI shown in Figs. 8 and 10, respectively, a dc equivalent circuit of the whole equalizer can be obtained, as shown in Fig. 11. The ideal transformer shown in Fig. 10 is replaced with an ideal multi-winding transformer with a turn ratio of N:1:1:1:1 for the cells, B_1–B_4, to be connected in series. The series connection of B_1–B_4 supplies the input current of $I_{in\text{-}ave}$ to the FFRI, in which $I_{in\text{-}ave}$ is divided into I_{mg} and I_T, and I_T is transferred to the secondary windings as I_{Ci} (i = 1…4). In the voltage multiplier, I_{Ci} is preferentially distributed to the least charged cell(s) with the lowest voltage in B_1–B_4. In other words, the power supplied to FFRI from the B_1–B_4 series connection is redistributed to the least charged cell(s) through the proposed voltage equalizer. In the course of the power redistribution, the voltage of the least charged cell(s) increases thanks to power redistribution by the voltage multiplier, whereas those of other cells decrease by supplying power to the FFRI. Ultimately, all the cell voltages are automatically unified.

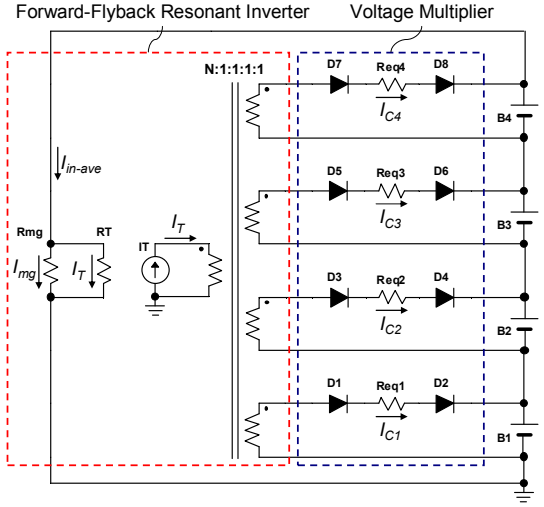
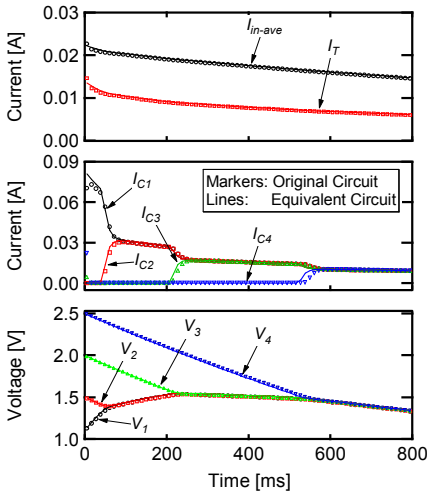


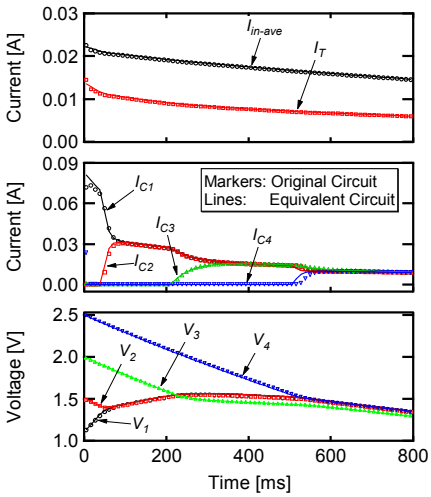
Fig. 11. DC equivalent circuit of the proposed voltage equalizer.

IV. Simulation Analysis for DC Equivalent Circuit

Simulation analyses were performed for both the original and derived dc equivalent circuits shown in Figs. 3 and 11, respectively, to validate the analysis procedure and derived equivalent circuit. The component values used in the simulation analyses were identical to those used for the prototype, as will be shown in Table I. The values of R_T and $R_{eq\text{-}i}$ were programmed according to (24) and (6), respectively, with k = 2.5. The snubber in the original circuit was modeled as a voltage source with 50 V. Capacitors with capacitance of 10 mF were used as energy storage cells of B_1–B_4. The simulation analyses were performed for four cells connected in series with a fixed D = 0.35 at f_S = 90 kHz from a voltage-imbalanced condition.



(a) C_i-matched condition.



(b) C_i-mismatched condition.

Fig. 12. Simulation results of original and derived dc equivalent circuits under (a) C_i-matched and (b) C_i-mismatched conditions.

Simulation results of the original and derived dc equivalent circuits are shown and compared in Fig. 12(a). The results matched well, verifying the analyses and derivation procedure presented in previous sections. At the beginning of the simulations, the least charged cell B_1 with the lowest initial voltage received the current from the equalizer and its voltage increased, while the voltages of other cells with higher initial voltages decreased as they supplied current to the equalizer. After V_1 overtook V_2, both increased at the same rate by receiving current from the equalizer because both V_1 and V_2 were the lowest. As the power redistribution progressed, all the cell voltages eventually became uniform at about 560 ms.

Similar simulation analyses were performed emulating a parameter-mismatched condition, where the parameters of C_3 only were severely mismatched as C_3 = 10 µF and r_3 = 350 mΩ, while others with C_i = 100 µF and r_i = 35 mΩ. Even under the severely mismatched condition, the results of the original and equivalent circuits matched well, verifying the modeling for equivalent resistance presented in Section III-C. At 220 ms, I_{C3} started to flow, meaning that i_{Cr} in the original circuit started to be distributed to C_3 in addition to C_1 and C_2. Therefore, the total capacitance viewed from C_r at that moment was the sum of C_1–C_3. Although C_3 was equal to C_r in this parameter-mismatched simulation, the resonant operation was unaffected because the total capacitance of C_1–C_3 was sufficiently larger than C_r, as mentioned in Section III-A. The voltage of B_3, V_3, which corresponded to the mismatched capacitor of C_3, was lower than the others due to the increased equivalent resistance of $R_{eq\text{-}i}$, as expressed by (6).

The simulation analysis for the original circuit took hours, whereas that for the equivalent circuit was completed instantly due to the lack of high-frequency operation. In addition, since the equalization behavior under parameter-mismatched condition can be precisely modeled, as shown in Fig. 12(b), the derived dc equivalent circuit is considered a powerful tool to quickly analyze the impacts of parameter mismatch on equalization performance.

V. Experimental Results

A. Prototype and Experimental Setup

To demonstrate the superior performance of the voltage equalizer using the FFRI to that using the FFI, two 6-W prototypes using each inverter were built for eight cells connected in series. Except for the resonant capacitor C_r, the same components were used for both prototypes; C_r was short-circuited for the FFI. The component values are listed in Table I, and a photograph of the prototype using the FFRI is shown in Fig. 13. Both prototypes were operated with a fixed D of 0.35 at f_S = 90 kHz.

The operation waveforms as well as characteristics including power conversion efficiencies under voltage-balanced and -imbalanced conditions were measured using the experimental setup shown in Fig. 14. The equalizers were powered by an external power supply, V_{ext}, while a variable resistor R_{var} was used instead of cells. By selecting the intermediate tap of X, current flow paths under the voltage-balanced condition can be emulated. Meanwhile, selecting the tap of Y emulates a voltage-imbalanced condition where V_1 is the lowest.

TABLE I
Component Values Used for the Prototype

Component	Value
C_1–C_8	Tantalum Capacitor, 100 µF, 35 mΩ
C_{out1}–C_{out8}	Ceramic Capacitor, 200 µF
D_1–D_{16}	Schottky Diode, DFLS220L, V_D = 0.45 V, R_D = 35 mΩ
C_r	Ceramic Capacitor, 10 µF
Q	N-Ch MOSFET, FDS86240, R_{on} = 35.3 mΩ
Transformer	N_1:N_2 = 36:3, L_{kg} = 9.8 µH, L_{mg} = 303 µH
Snubber	R_{SN} = 150 kΩ, C_{SN} = 20 nF

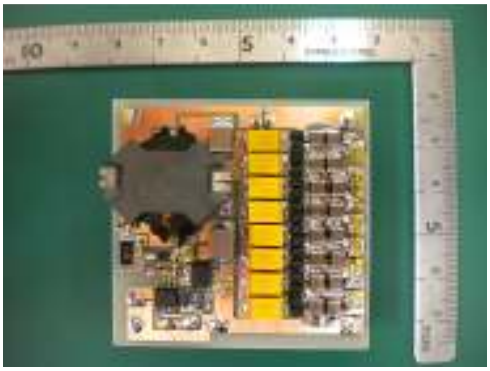


Fig. 13. A photograph of 6-W prototype of the proposed equalizer using FFRI for eight cells connected in series.

B. Measured Waveforms and Power Conversion Efficiencies

Measured key operation waveforms of the equalizers using the FFI and FFRI under voltage-balanced and -imbalanced conditions are shown in Figs. 15 and 16. In both equalizers and under both conditions, switches were turned on at ZCS. As discussed in Section III-B, i_Q in the FFI consistently increased during the on-period, while its value at turn-off transition considerably exceeded that in the FFRI shown in Fig. 16. $i_{Secondary}$ and i_{Cr} linearly changed in the off periods, and after they reached zero, oscillations in v_{DS} caused by the resonance between L_{mg} and MOSFET's output capacitance were observed.

Somewhat different current waveforms were observed under voltage-balanced and -imbalanced conditions, in both prototypes. These differences are considered attributable to the

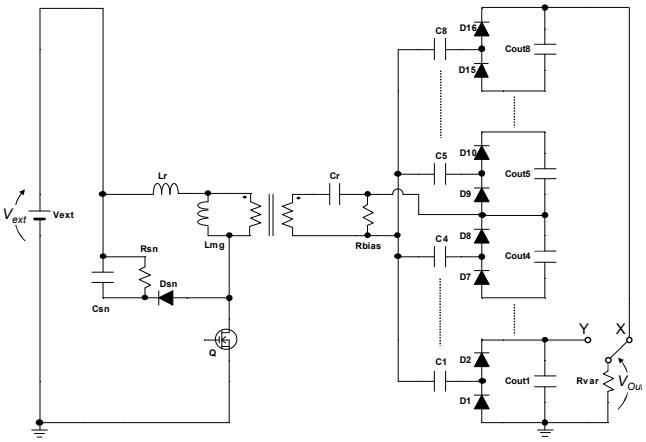
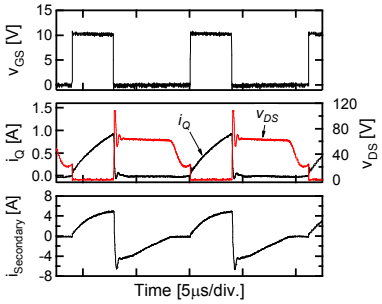
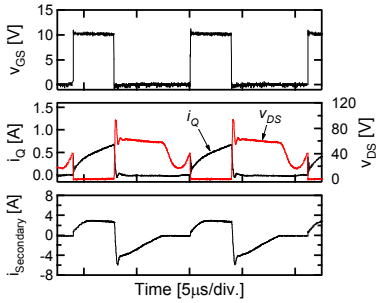


Fig. 14. Experimental setup for characteristic measurement.

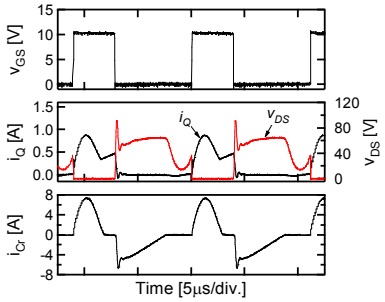


(a) Voltage-balanced condition.

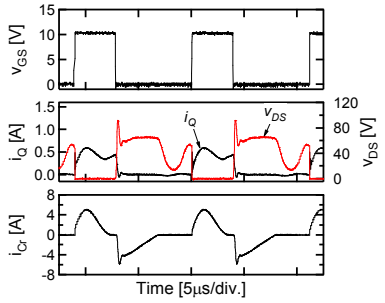


(b) Voltage-imbalanced condition.

Fig. 15. Measured waveforms of the equalizer using FFI under (a) voltage-balanced and (b) voltage-imbalanced conditions.



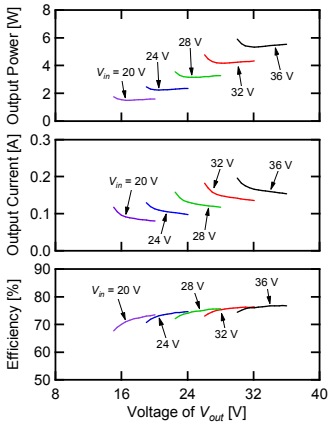
(a) Voltage-balanced condition.



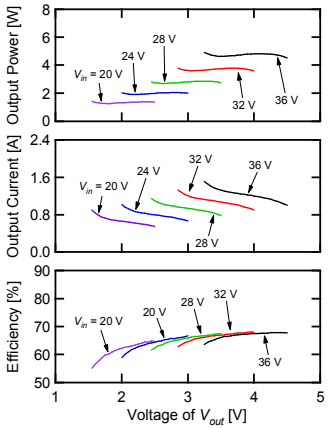
(b) Voltage-imbalanced condition.

Fig. 16. Measured waveforms of the equalizer using FFRI under (a) voltage-balanced and (b) voltage-imbalanced conditions.

current concentration in the voltage multiplier. Under voltage-balanced conditions, the current supplied from the secondary winding (i_{Cr} and $i_{Secondary}$ shown in Fig. 1) is distributed to all capacitors and diodes (as shown in Fig. 5), whereas the current is concentrated on C_1 and D_1–D_2 under voltage-imbalanced condition, producing significant voltage drops in r_l and r_D that affect operation as well as current waveforms of the FFI and FFRI.



(a) Voltage-balanced condition.

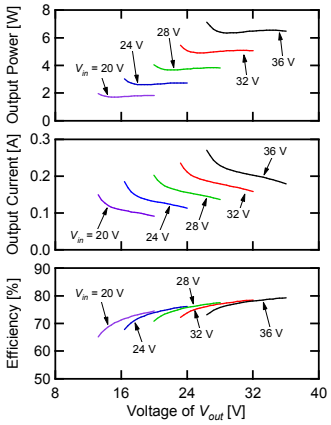


(b) Voltage-imbalanced condition.

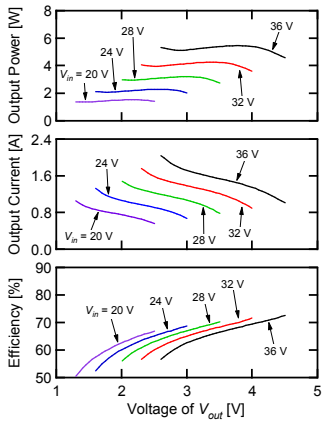
Fig. 17. Measured efficiencies and output characteristics of the equalizer using FFI under (a) voltage-balanced and (b) voltage-imbalanced conditions.

The measured power conversion efficiencies and output characteristics of the equalizers using FFI and FFRI at various input voltages are shown in Figs. 17 and 18. The efficiencies under the voltage-imbalanced conditions were lower than those under the voltage-balanced conditions for both equalizers. This is because, under the voltage imbalanced conditions, the current concentrated on C_1 and D_1–D_2 in the voltage multiplier, increasing Joule losses in r_l and r_D. The equalizer using the FFRI showed higher efficiencies; the measured peak efficiencies at V_{in} = 36 V under voltage-balanced conditions, for example, were 75–80% and 72–77% for equalizers using FFRI and FFI, respectively. The superior efficiency of the equalizer using the FFRI is considered due to the reduced turn-off switching loss and snubber loss, as explained in Section III-B.

These measured efficiencies were somewhat higher than those of conventional equalizers using different inverters to drive the voltage multiplier [32], [33]. However, given that efficiencies are dependent on various conditions, such as switching frequency, voltage range, number of cells connected in series, component selections, etc., the proposed voltage equalizers in terms of efficiency are considered comparable with conventional ones. This conclusion can also be obtained from that fact that the forward voltage drop of each diode in the voltage multiplier takes a significant portion of the relatively



(a) Voltage-balanced condition.



(b) Voltage-imbalanced condition.

Fig. 18. Measured efficiencies and output characteristics of the equalizer using FFRI under (a) voltage-balanced and (b) voltage-imbalanced conditions.

low output voltage (or cell voltage), collectively becoming a significant and major loss, as mentioned in Section II-B. If the loss in the voltage multiplier can be assumed dominant over that in the inverter, efficiencies would be insensitive to the type of inverter used to drive the voltage multiplier.

C. *Equalization for Series-Connected SCs*

An experimental equalization test using the prototype with the FFRI was performed for eight SCs connected in series, each with capacitance of 1500 F at a rated charge voltage of 2.5 V. Voltages of SCs were initially imbalanced within the range of 1.1–2.5 V. A data logger (NR-HA08, KEYENCE) with the least significant bit resolution of 0.31 mV was used to record the cell voltages during the equalization.

The experimental equalization profiles of eight SCs connected in series are shown in Fig. 19. Similar to the simulation results shown in Fig. 12, cell voltages with high initial voltages decreased by supplying power to the equalizer, while that with the low initial voltage increased by receiving the power distributed by the equalizer. All the cell voltages gradually converged and eventually became nearly uniform. The standard deviation declined to as low as 5 mV at the end of the equalization test, successfully demonstrating the equalization performance.

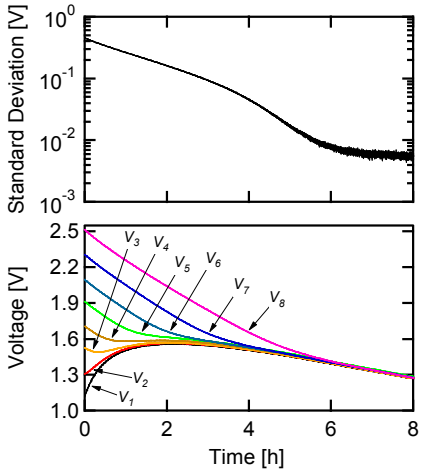


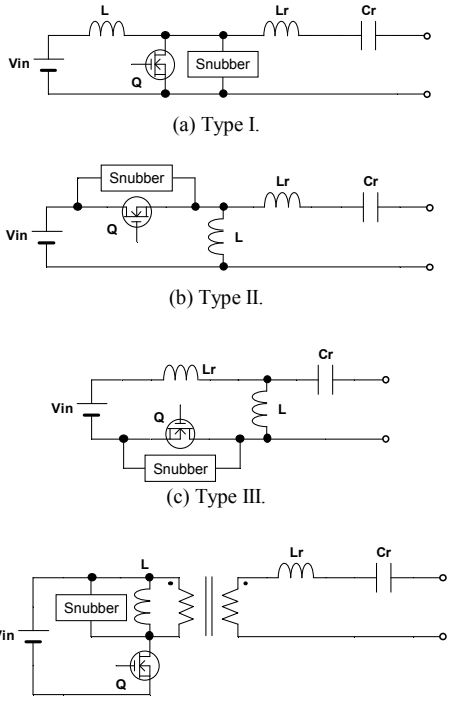
Fig. 19. Experimental equalization profiles of eight SCs connected in series.

The cell voltages continued decreasing, even after they had been sufficiently equalized, because the equalizer was still operating and meaninglessly circulating energy, resulting in power conversion loss in the equalizer. Therefore, if loss minimization is required, the equalizer should be disabled when not needed, and voltage-sensing for each cell and management system would be necessary to enable/disable the equalizer.

VI. Extended Topologies —Single-Switch Resonant Equalization Charger

A. *Feasible Resonant Input Cells*

The FFRI shown in Fig. 1(b) can be extended as feasible resonant input cells, as either nonisolated or isolated versions. The feasible input cells are listed in Fig. 20 and their



(a) Type I.

(b) Type II.

(c) Type III.

(d) Type IV.

Fig. 20. Feasible resonant input cells.

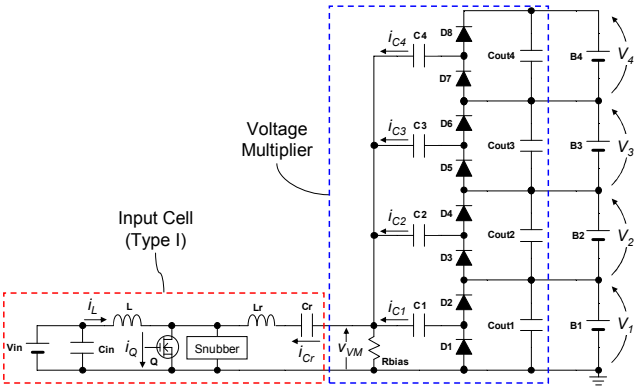


Fig. 21. Nonisolated single-switch resonant equalization charger.

fundamental operation principle is identical to that of the FFRI shown in Fig. 1(b); L_r and C_r resonate and L stores energy during the on-period, while the stored energy in L is discharged in the off-period. The input cells shown in Figs. 20(b) and (c) correspond to the nonisolated versions of the cells shown in Fig. 20(d) and the FFRI shown in Fig. 1(b), respectively.

By combining one of the resonant input cells and the voltage multiplier shown in Fig. 2, a single-switch equalization charger, which is basically a charger with an equalization function, can be derived, as explained in the following subsection. Nonisolated input cells cannot be used for voltage equalizers because, as mathematically expressed in Section III-D, the transformer is necessary to limit current in voltage equalizers where the difference between input and output voltages (i.e. V_{in} and V_i) tend to be significant with increasing number of cells connected in series. Meanwhile, isolated input cells shown in Figs. 1(b) and 20(d) can be used for both equalizers and equalization chargers.

B. Nonisolated Single-Switch Resonant Equalization Charger

By combining a resonant input cell and the voltage multiplier, a single-switch resonant equalization charger can be derived. A representative topology using the resonant input cell shown in Fig. 20(a) is depicted in Fig. 21. The fundamental operation closely resembles that of the equalizer explained in Section III-D, except power is supplied by an external power source in the equalization charger. The equalizer presented in Section III relies on the DCM operation to limit current, and open-loop control is feasible. However, since the equalization charger is basically a charger, feedback control is imperative for regulating charge current and voltage.

With the derived equalization charger, a charger and equalizer can be integrated, simplifying a charging system. However, the equalization charger tends to be less efficient than conventional chargers having a single high-voltage output [41], [42] because of collective diode losses in the voltage multiplier and snubber loss. Hence, the equalization charger is considered suitable for low power applications and/or auxiliary chargers that complement main chargers and equalize cell voltages.

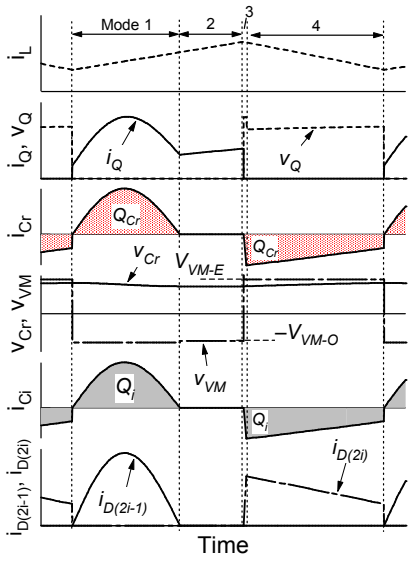


Fig. 22. Key operation waveforms of the resonant equalization charger.

C. Analysis and Modeling for Resonant Equalization Charger

The resonant equalization charger operates in either DCM or continuous conduction mode (CCM). In general, CCM operation is advantageous over DCM in terms of reducing peak current as well as Joule losses. The theoretical key operation waveforms of the resonant equalization charger in CCM are shown in Fig. 22. These waveforms are very similar to those shown in Fig. 4, and the operation of the voltage multiplier can be expressed using the same equations developed in Section III-C.

The average voltage of inductors under a steady-state condition is zero, and due to the bias resistor R_{bias} connected to the input of the voltage multiplier, the average voltage of C_r, V_{Cr}, is equal to V_{in} in the resonant equalization charger shown in Fig. 21. Assuming the voltage of C_r to be constant and its variation sufficiently smaller than that in v_{VM}, as shown in Fig. 22, the input voltage of the voltage multiplier during Mode O, V_{VM-O}, can be approximated as

$$V_{VM-O} = V_{Cr} = V_{in}. \tag{25}$$

Neglecting the voltage drop in $R_{eq\text{-}i}$ and substituting (25) into (5) yields the voltage multiplier's input voltage during Mode E,

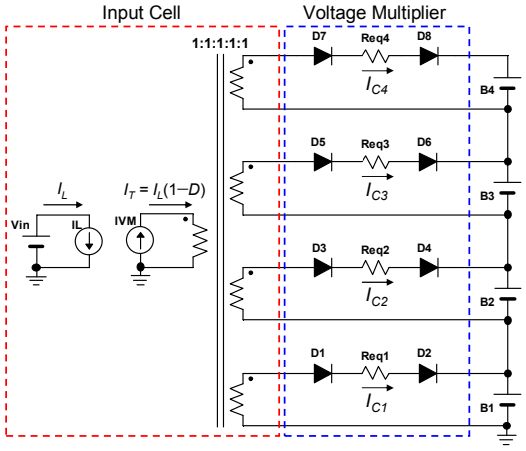


Fig. 23. DC equivalent circuit of the resonant equalization charger.

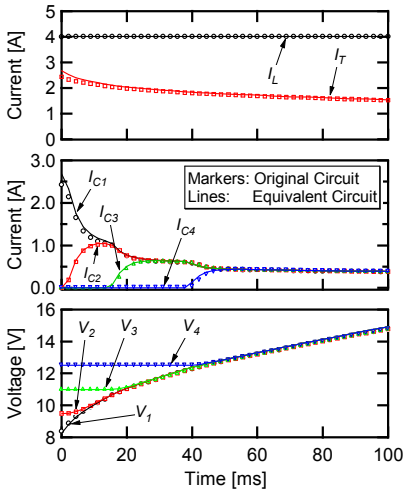


Fig. 24. Simulation results of original and derived dc equivalent circuits.

$V_{VM\text{-}E}$, as

$$V_{VM-E} = V_i + 2V_D - V_{in}\,. \tag{26}$$

From the volt-second product on L using (25) and (26),

$$V_i = \frac{V_{in}}{1-D} - 2V_D\,. \tag{27}$$

In the resonant equalization charger shown in Fig. 21, the average input current, $I_{in\text{-}ave}$, is equal to the average inductor current of I_L, which is determined according to the controlled charging current. Meanwhile, the voltage multiplier in the resonant equalization charger can be modeled equivalently as presented in Section III-C. Since $I_{Ci} = Q_i f_S$ (see Section III-C), transformation of (7) for the voltage multiplier in the resonant equalization charger produces

$$I_{VM} = f_S \sum_i^n Q_i = f_S Q_{Cr} = I_L(1-D), \tag{28}$$

where Q_{Cr} is the charge delivered through C_r as designated in Fig. 22. Here, the snubbering period of Mode 3 is neglected for simplicity.

From (28) and the equivalent circuit of the voltage multiplier shown in Fig. 4, the dc equivalent circuit of the resonant equalization charger can be derived as illustrated in Fig. 23. An ideal transformer with a turn ratio of 1:1:1:1:1 is used for the cells to be connected in series.

Similar to Section IV, simulation analyses for both the original and derived dc equivalent circuits shown in Figs. 21 and 23, respectively, were performed for the four capacitors of B_1–B_4 connected in series; each with capacitance of 10 mF. Simulation circuits were modeled using component values for the experiment (see Table II in the following subsection). The simulations were performed with V_{in} = 6.0 V at f_S = 90 kHz from an initially-voltage-imbalanced condition, and cells were charged with a CIC (constant input current) charging scheme [34] of 4.0 A.

Simulation results are shown and compared in Fig. 24. The results matched well, successfully verifying the derived dc equivalent circuit. Similar to the equalizer, charging power was preferentially supplied to B_1, the cell with the lowest initial voltage. Meanwhile, voltages of higher initial voltage (i.e. V_2–V_4) remained constant until V_1 overtook because the charging power was supplied by the external voltage source of V_{in}, not by the series connection of B_1–B_4.

D. Experimental Results

A 20-W prototype of the equalization charger shown in Fig. 21 was built for four SC modules connected in series. A photograph of the prototype and component values are shown in Fig. 25 and Table II, respectively. The measured efficiency at 20 W was approximately 85%. SC modules, each with capacitance of 220 F at a rated charge voltage of 15.0 V, were used. The input voltage V_{in} was 6.0 V, and the equalization charger was operated at f_S = 90 kHz with a CIC–CV (constant input current–constant voltage) charging scheme [34] of 4.0 A and 14.5 V. The modules were charged until the input current of I_{in} tapered to 0.3 A during the CV charging period.

The resulting charging profiles are shown in Fig. 26. Measured key waveforms at t = 0 and 40 min, at which module voltages were imbalanced and balanced, respectively, are also shown in Fig. 27 — duty cycles were varied according to module voltages, while I_L was controlled to be 4.0 A by the CIC charging scheme. Similar to the simulation results shown in Fig. 24, at the beginning of the charging, the module with the lowest initial voltage, B_1, received the current of I_1 and its voltage V_1 increased. As V_1 increased and overtook other voltages, other modules started receiving current from the charger one by one, whereupon their voltages also increased. All the module voltages of V_1–V_4 as well as the current of I_1–I_4 became nearly uniform 25 min after the beginning of the charging. After V_1–V_4 reached the CV charging voltage level of 14.5 V, the voltages were kept constant and the charging current started to be tapered by the CV charging scheme. The standard deviation in module voltages consistently decreased during the CIC charging period.

TABLE II
COMPONENT VALUES FOR THE RESONANT EQUALIZATION CHARGER.

Component	Value
C_1–C_4	Tantalum Capacitor, 94 µF, 22.5 mΩ
C_{out1}–C_{out4}	Ceramic Capacitor, 66 µF
D_1–D_8	Schottky Diode, STPS1150, V_D = 0.71 V, R_D = 25 mΩ
C_r	Ceramic Capacitor, 10 µF
L	33 µH
L_r	150 nH
Q	N-Ch MOSFET, HAT2260, R_{on} = 9.2 mΩ
Snubber	R_{SN} = 4.7 kΩ, C_{SN} = 20 nF

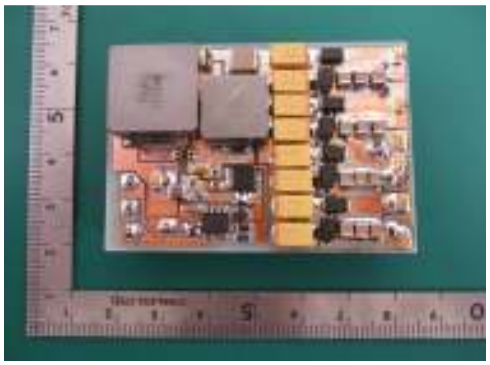


Fig. 25. A photograph of 20-W prototype of the resonant equalization charger for four modules connected in series.

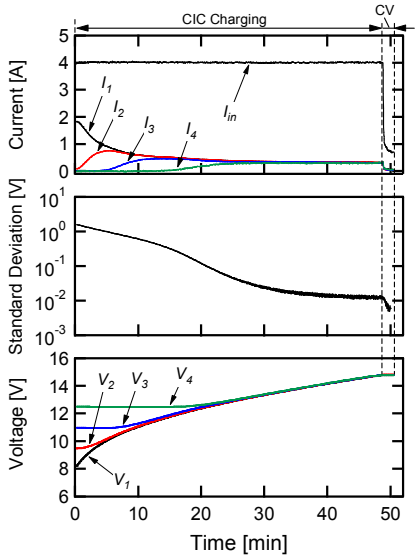


Fig. 26. Experimental charging profiles of four SC modules connected in series.

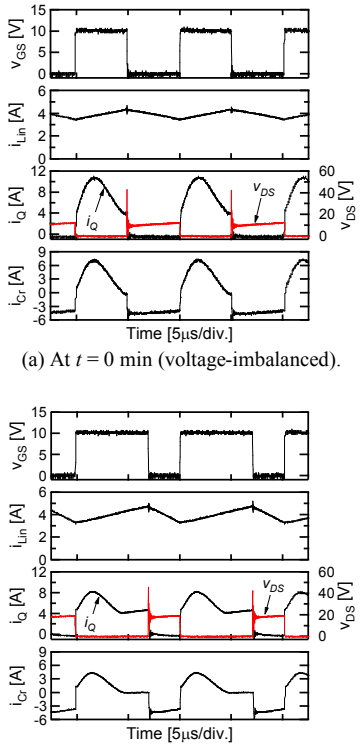
Once the charging shifted to the CV charging period, the standard deviation declined further due to the tapered charging current; the lower the current, the smaller will be the voltage imbalance due to the minor parameter mismatch, as indicated by (8).

VII. Conclusions

Single-switch single-transformer voltage equalizers using an FFI/FFRI with a voltage multiplier have been proposed in this paper. The required switch count can be minimized without impairing modularity by the proposed equalizer due to the single-switch circuitry with no need of a multi-winding transformer. The proposed equalizer using the FFRI achieves higher efficiency than that using the FFI because the resonant operation reduces turn-off switching loss as well as snubber loss. The FFRI and voltage multiplier were separately analyzed in detail, and a dc equivalent circuit of the equalizer as a whole, with which equalization characteristics can be quickly simulated without lengthy simulation analysis, was derived based on the mathematical analyses.

Two 6-W prototypes of the proposed equalizer using the FFI or FFRI for eight cells connected in series were built and tested. The FFRI-based equalizer outperformed the FFI-based one in terms of power conversion efficiency, thanks to the reduced switching loss as well as snubber loss. An equalization test for eight SCs connected in series was performed using the FFRI-based equalizer from an initially-voltage-imbalanced condition. The voltage imbalance was gradually eliminated and all the cell voltages were eventually unified, demonstrating the equalization performance of the proposed single-switch equalizer.

The FFRI was extended as a "resonant input cell". By combining one of the resonant input cells and a voltage multiplier, a single-switch resonant equalization charger, which is basically a charger with an equalization function, was also derived. A 20-W prototype of the resonant equalization charger



(a) At t = 0 min (voltage-imbalanced).

(b) At t = 40 min (voltage-balanced).

Fig. 27. Measured waveforms of the resonant equalization charger at t = (a) 0 min (voltage-imbalanced condition) and (b) 40 min (voltage-balanced condition).

was built, and a charging test for four SC modules connected in series was also performed from a voltage-imbalanced condition. All the modules were charged to the uniform voltage level at the end of the charging test, verifying the performance of the extended topology.

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