Double-Switch Equalizer Using Parallel- or Series-Parallel-Resonant Inverter and Voltage Multiplier for Series-Connected Supercapacitors

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***Abstract*— A double-switch cell voltage equalizer using a parallel-resonant-inverter (PRI) or series-parallel-resonant inverter (SPRI) and voltage multiplier is proposed for series-connected supercapacitors (SCs), such as electric double-layer capacitors (EDLCs) and lithium-ion capacitors. The double-switch operation without the need for a multi-winding transformer offers simpler circuitry as well as better modularity than conventional equalizers requiring multiple switches and/or a multi-winding transformer. Furthermore, the inherent constant current characteristic of the PRI/SPRI at a fixed frequency, not only removes the need for feedback control to limit currents under desired levels but the proposed equalizer can also operate safely, even when some cell voltage is 0 V. Detailed operation analyses were separately performed for the voltage multiplier and PRI/SPRI, and a dc equivalent circuit for the proposed equalizer was mathematically derived. A 10-W prototype for 12 cells connected in series was built, and an experimental equalization test was performed for EDLCs from an initially-voltage imbalanced condition. Voltage imbalance of the series-connected EDLCs was successfully eliminated by the equalizer, demonstrating the equalization performance of the proposed equalizer.**

***Index Terms*— Battery, equalizer, parallel-resonant inverter, series-parallel-resonant inverter, supercapacitor, voltage imbalance, voltage multiplier.**

I. Introduction

Energy storage plays an important role in various applications, including portable electronic devices, electric vehicles, renewable energy systems, etc. Secondary battery technologies are the most popular energy storage medium, and their role is rapidly increasing especially since the advent of lithium-ion batteries that offer the highest specific energy among secondary battery technologies.

Alongside, significant attentions have been paid to supercapacitors (SCs). SCs, including electric double-layer capacitors (EDLCs) and lithium-ion capacitors (LICs) [1] that are namely a hybrid capacitor combining features of both conventional EDLCs and lithium-ion batteries, are an energy storage device advantageous over traditional secondary batteries in terms of service life, power capability, and temperature tolerance. However, since the specific energy of SCs is relatively lower than that of secondary batteries, uses of SCs has mainly been limited to high-power applications where SCs are used as power buffers to complement secondary batteries and/or other power generators. Vigorous research and development efforts to achieve higher specific energy and even longer service life are underway to expand their applications. As the specific energy of SCs steadily increases and long service life over wide temperature range is factored in, SC technologies have been considered as a potential alternative energy storage source to traditional secondary batteries [2],[3].

Generally, series-connected energy storage cells suffer from cell voltage imbalances that may lead to overcharging and over-discharging of cells; the most and least charged cells in a voltage-imbalanced series connection may be overcharged and over-discharged during charging and discharging processes, respectively. Nonuniformity is individual cell properties of series-connected cells, in terms of capacitance, internal impedance, self-discharge, is the major reason triggering voltage imbalance. Another cause that cannot be controlled in manufacturing processes is a temperature gradient among cells in practical use that exacerbate nonuniform self-discharging. Accordingly, cell voltage equalization is essential for series-connected cells to ensure years of service life.

A large variety of cell voltage equalization techniques have been proposed, demonstrated, and implemented for SCs and lithium-ion batteries. Cell voltage equalizers using multiple bidirectional dc-dc converters, such as buck-boost converters [4]–[8], switched capacitor converters [9]–[17], and converters using transformers [18]–[20], are among the most common approaches. However, the number of switches required in these equalizers is proportional to the number of series connections, meaning the circuit complexity is prone to significantly increase with the number of series connections. Cell voltage equalizers based on a single isolated converter and selection switches can reduce the number of passive components dramatically and are considered suitable for applications requiring numerous series connections, such as electric vehicles [21]–[26], but many switches are still required in proportion to the number of series connections. In addition, an intelligent management system is also required to determine a target cell ―the least- or

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most-charged cell — for the equalizer to execute equalization, which makes these equalizers less attractive for small-scale energy storage systems, where simple electronics are preferable. Equalizers using multi-winding transformers can be configured with fewer switches and passive components [27]–[30]. However, multi-winding transformers must be designed so that parameters among multiple secondary windings are strictly matched [31],[32]. The transformer design becomes a daunting challenge with the rising number of secondary windings, impeding the modularity of these equalizers and rendering them unsuitable for applications requiring numerous series connections. Single-switch equalizers using multi-stacked buck-boost converters, meanwhile, can be built without a multi-winding transformer, hence allowing both simplified circuitry and good modularity to be achieved [33]. However, the multiple inductor requirement is the major drawback; the size of these equalizers is prone to be bulky, especially for applications requiring numerous series connections. Single-switch single-transformer equalizers and equalization chargers using voltage multipliers have also been proposed [34],[35]. Although the circuitry can be simplified at a reasonable size, the occurrence of high capacitive inrush currents poses issues, not only in terms of the current stresses of devices but also EMI.

We have proposed a double-switch single-transformer equalizer using a half-bridge inverter and voltage multiplier for series-connected SCs [36]. The energy of the series-connected SCs is supplied to the half-bridge inverter, and then transferred to the voltage multiplier, which preferentially redistributes the energy to an SC having the lowest voltage. Although the required number of switches is doubled (i.e. two) compared to those in [34],[35], the leakage inductance of the transformer prevents the occurrence of capacitive inrush currents, making this equalizer more compatible with any applications. However, since the half-bridge inverter is basically a voltage source which generates a square wave, and likewise SCs, currents in the equalizer may be excessive; a current between two voltage sources is prone to be large when a voltage difference between two sources is considerable. The considerable voltage difference is very likely because SC voltages vary significantly, typically 0–3.0 V and 2.0–4.0 V for EDLCs and LICs, respectively, and EDLCs at 0 V are equivalent to a short-circuit load. Given that high safety must be ensured in energy storage applications, protection against excessive current is indispensable for equalizers. However, an increase in component count and complexity due to an additional protection circuit may contrarily impair reliability. Since SCs are inherently a long-life energy storage device, peripheral circuits including equalizers are preferred to be as simple as possible to ensure high reliability. Therefore, equalizers that intrinsically possess protection against excessive current are considered desirable for SCs, although no previous work has focused on this issue.

In this paper, a double-switch equalizer using a parallel-resonant inverter (PRI) or series-parallel-resonant inverter (SPRI) and voltage multiplier is proposed for series-connected SCs. The proposed equalizer can be derived from a combination of a PRI/SPRI and a voltage multiplier. The PRI/SPRI provides an inherent constant current characteristic even at a fixed frequency, while the voltage multiplier automatically equalizes cell voltages. The double-switch configuration without the need for a multi-winding transformer offers simplified circuitry and good modularity. In addition, the proposed equalizer can operate safely, even when some SC voltage is 0 V, because the inherent constant current characteristic of the PRI/SPRI automatically limits currents under desired levels. The proposed equalizer is best suitable for SCs but also can be used as an equalizer for series-connected lithium-ion batteries.

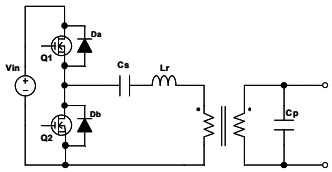
The circuit derivation and configuration of the proposed equalizer are described in Section II, while Section III separately analyzes the voltage multiplier and PRI/SPRI, whereupon a dc equivalent circuit of the proposed equalizer is mathematically derived. In Section IV, design guide is presented by giving an example of a 10-W equalizer using a PRI. In Section V, simulation-based equalizations are performed for both the original and derived dc equivalent circuits to verify the equalization characteristic as well as the derived equivalent circuit. A 10-W prototype using a PRI for 12 cells connected in series is built, and an experimental equalization test is performed for series-connected EDLCs with the prototype in Section VI. In Section VII, the proposed equalizer is compared to conventional equalizers in terms of circuit complexity, modularity, and size, and major benefits of the proposed equalizer are summarized.

II. Double-Switch Equalizer Using a Parallel-Resonant or Series-Parallel-Resonant Inverter and Voltage Multiplier

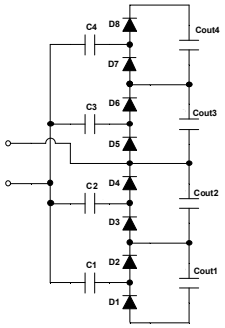
A. Parallel-Resonant/Series-Parallel-Resonant Inverter and Voltage Multiplier

The proposed cell voltage equalizer is essentially the combination of a PRI/SPRI and voltage multiplier. A conventional PRI/SPRI is shown in Fig. 1(a). With a parallel-resonant capacitor, C_p, on the transformer secondary side, the leakage inductance of the transformer can be incorporated into the resonant inductor, L_r. For the circuit shown in Fig. 1(a) to operate as a PRI, the capacitance of the series-resonant capacitor C_s, C_s, must considerably exceed that of C_p, C_p, so that C_s acts as a dc blocking capacitor. Meanwhile, if C_s and C_p are comparable, the circuit operates as an SPRI. The detailed operation analysis for the PRI/SPRI is made in Section III-C.

A 4x voltage multiplier, which consists of coupling capacitors C_1–C_4, smoothing capacitors C_{out1}–C_{out4}, and diodes D_1–D_8, is shown in Fig. 1(b) as a representative configuration. As ac voltage/current waves are fed to the voltage multiplier, voltages of C_{out1}–C_{out4} automatically become uniform. Section III-B mathematically analyzes the operation of the voltage multiplier when used with a PRI/SPRI.



(a) PRI/SPRI.



(b) Voltage multiplier.

Fig. 1. (a) Conventional PRI/SPRI with C_p on the transformer secondary side and (b) voltage multiplier.

B. Proposed Equalizer

The proposed cell voltage equalizer using a PRI/SPRI and voltage multiplier for four cells connected in series is shown in Fig. 2. The output of the PRI/SPRI is connected to the input of the voltage multiplier. Energy storage cells, B_1–B_4, are connected to C_{out1}–C_{out4} in parallel. The series connection of B_1–B_4 is connected to the input of the PRI/SPRI for power circulation and voltage equalization. The series connection of B_1–B_4 powers the PRI/SPRI, through which the supplied power is transferred to the voltage multiplier in ac form. Subsequently, the voltage multiplier rectifies the ac power and redistributes the power to B_1–B_4. In the course of the power circulation, the voltages of B_1–B_4, V_1–V_4, are automatically equalized by the voltage multiplier. This automatic equalization is applicable to not only series-connected SCs but also lithium-ion batteries because the voltage multiplier operates so that all cell voltages become uniform, regardless of what cells are used, as mathematically detailed in Section III-B. However, the proposed equalizer is considered best suitable for series-connected SCs because of the inherent constant current characteristic that realizes the safety operation even when some cell voltage is 0 V, as discussed in Section III-C.

In this section, the proposed equalizer using the voltage multiplier for four cells connected in series was shown as an example. However, by changing the connection, the voltage multiplier can be composed of any arbitrary number, including odd number, of cells connected in series. For example, in the previous work for the single-switch multi-output charger [35] that uses the similar voltage multiplier, operation analysis, simulation, and experiments were performed using the voltage multiplier for three EDLC modules connected in series, although the characteristic of the voltage multiplier in [35] differs from that in the proposed equalizer in this paper.

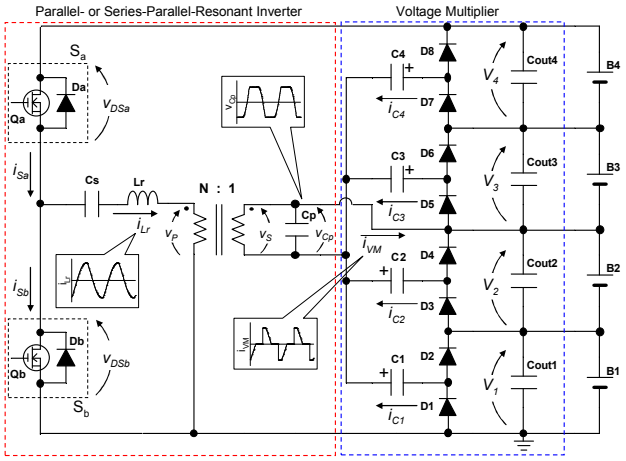


Fig. 2. Double-switch equalizer using PRI/SPRI and voltage multiplier for four cells connected in series.

III. Operating Analysis

Key waveforms and operation modes of the proposed equalizer are first explained, followed by separate analyses for the voltage multiplier and the PRI/SPRI, respectively. The voltage equalization mechanism of the voltage multiplier and the inherent constant current characteristic of the PRI/SPRI are mathematically explained. DC equivalent circuits for both the voltage multiplier and the PRI/SPRI are separately derived, whereupon, by combining these equivalent circuits, a dc equivalent circuit for the whole equalizer is obtained.

A. Operation Waveforms and Current Flows

Similar to conventional resonant inverters, the PRI/SPRI in the proposed equalizer is operated above resonance, whereby the resonant circuit represents the inductive characteristic and switches are turned-on at zero voltage, thus achieving zero voltage switching (ZVS). The theoretical key operation waveforms and current flow directions of the proposed equalizer under a voltage-balanced condition are shown in Figs. 3 and 4, respectively. Waveforms in Fig. 3 are illustrated by assuming that all components in the circuits are ideal and the

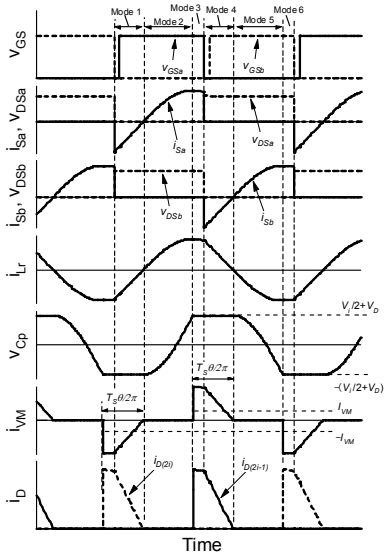
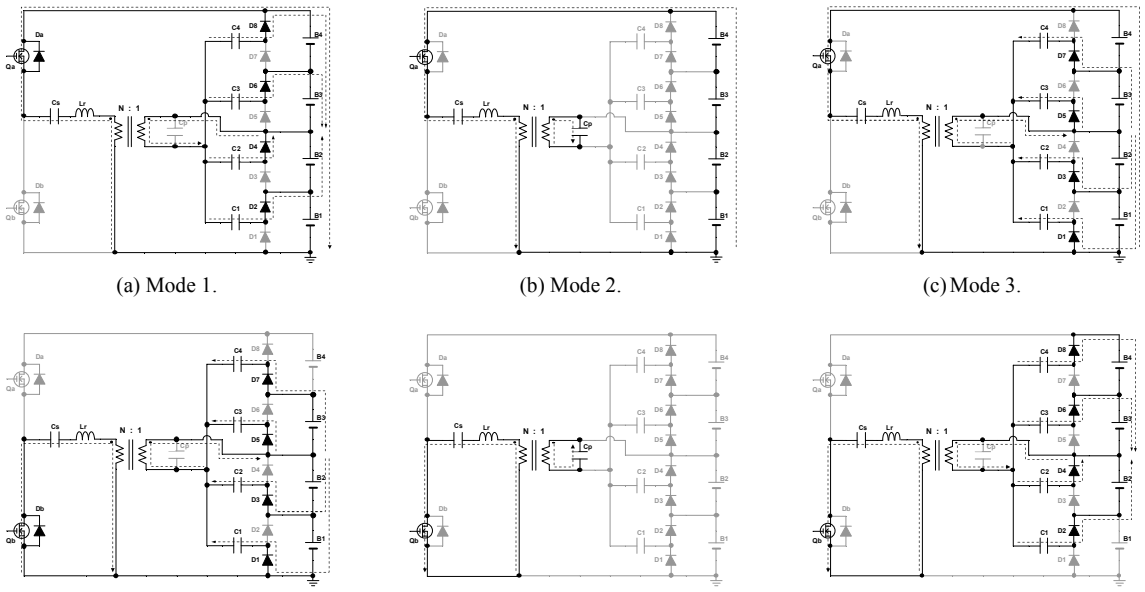


Fig. 3. Key operation waveforms under voltage-balanced condition.



(a) Mode 1. (b) Mode 2. (c) Mode 3.

(d) Mode 4. (e) Mode 5. (f) Mode 6.

Fig. 4. Current flow directions.

capacitances of C_1–C_4 are sufficiently large to ensure their constant voltages. For the sake of clarity, the smoothing capacitors, which are connected to cells in parallel, are not illustrated in Fig. 4. Either the PRI or SPRI is used, the operation of the proposed equalizer can be explained with the same waveforms and current flow directions. The operation of the proposed equalizer resembles that of a PRI/SPRI with a capacitive output filter [37]–[39] because $C_{out\text{-}i}$ and B_i ($i = 1 \ldots 4$) together act as a capacitive output filter. A detailed operation analysis of the PRI/SPRI in the proposed equalizer is made in Section III-C.

In mode 1, the voltage of C_p, v_{Cp}, is clamped to $-(V_i/2 + V_D)$, where V_D is the forward voltage drop of diodes, and the current of the voltage multiplier, i_{VM}, flows through even-numbered diodes, $D_{(2i)}$. L_r and C_s resonate, and the current of L_r, i_{Lr}, flows through the channel of Q_a or its anti-parallel diode, D_a. Before i_{Lr} reaches zero, the gating signal for Q_a, v_{GSa}, is applied to turn on Q_a at zero voltage.

When i_{Lr} reaches zero, mode 2 begins. As $D_{(2i)}$ ceases to conduct and C_p joins the resonant operation, v_{Cp} increases. In this mode, C_i in the voltage multiplier is neither charged nor discharged.

After v_{Cp} increases to the clamp level of $V_i/2 + V_D$, mode 3 begins and i_{VM} starts to flow through the odd-numbered diodes, $D_{(2i-1)}$. Since C_p is clamped and no current flows through it in this mode, C_p does not participate the resonant operation — only L_r and C_s resonate. As v_{GSa} is removed, the operation moves to mode 4. Modes 4–6 are symmetrical to modes 1–3.

Under the voltage-balanced condition shown in Fig. 4, i_{VM} is equally distributed to each C_1–C_4. Under voltage-imbalanced conditions, on the other hand, i_{VM} is likely to flow through only one of C_1–C_4, depending on voltage-imbalanced conditions. Waveforms under voltage-imbalanced conditions are basically similar to those shown in Fig. 3, although the current concentration in the voltage multiplier slightly influences the operation of the PRI/SPRI in practical circuit, as experimentally demonstrated in Section VI-B.

B. Modeling for the Voltage Multiplier

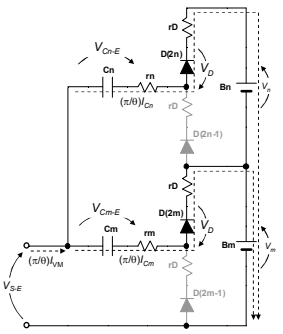
In this subsection, the voltage multiplier is analyzed on the premise that impedances of smoothing capacitors, which are connected to cells in parallel as shown in Fig. 2, are negligibly small.

As shown in Figs. 3 and 4, the PRI/SPRI provides the voltage multiplier with a current of i_{VM} only during C_p is clamped. In this subsection, the operation analysis for the voltage multiplier is made by simplifying its operation; the voltage multiplier operates with two modes, E and O, featuring even- and odd-numbered diode-conducting periods, as shown in Figs. 5(a) and (b), respectively. For clarity, a voltage multiplier for two cells only (B_m and B_n) is depicted in Fig. 5, and smoothing capacitors for B_m and B_n are not illustrated for the sake of clarity. The length of each mode is $T_S\theta/2\pi$, as designated in Fig. 3, where T_S is the switching period and θ is the conduction angle of the diodes. The average current of i_{VM} over the C_p-clamping period is given by $I_{VM}\pi/\theta$, where I_{VM} is the average current of i_{VM} over a half switching period (see Fig. 3).

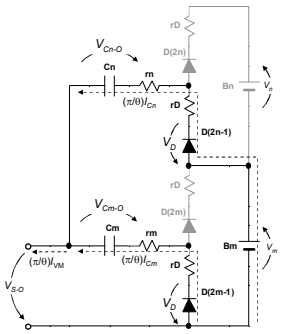
The voltage of the transformer secondary winding during mode E, $V_{S\text{-}E}$, which corresponds to the input voltage of the voltage multiplier as shown in Fig. 5(a), is expressed as

$$\begin{aligned} V_{S-E} &= V_m - V_{Cm-E} + V_D + \frac{\pi}{\theta} I_{Cm}\left(r_m + r_D\right) \\ &= V_m + V_n - V_{Cn-E} + V_D + \frac{\pi}{\theta} I_{Cn}\left(r_n + r_D\right) \end{aligned}, \tag{1}$$

where V_i ($i = m$ or n) is the voltage of B_i, $V_{Ci\text{-}E}$ is the voltage of C_i during mode E, I_{Ci} is the average current of C_i over a half switching period, r_i is the ESR of C_i, and r_D is the resistance of the diodes. Similarly, from Fig. 5(b), the voltage of the secondary winding during mode O, $V_{S\text{-}O}$, is



(a) Mode E (even-numbered diodes are on).



(b) Mode O (odd-numbered diodes are on).

Fig. 5. Simplified operation modes for the voltage multiplier.

$$V_{S-O} = V_{Cm-O} + V_D + \frac{\pi}{\theta} I_{Cm}\left(r_m + r_D\right) = -V_m + V_{Cn-O} + V_D + \frac{\pi}{\theta} I_{Cn}\left(r_n + r_D\right), \quad (2)$$

where $V_{Ci\text{-}O}$ is the voltage of C_i during mode O.

As shown in Figs. 4 and 5, currents flowing through inner cells (B_2–B_3 in Fig. 4, and B_m in Fig. 5) are larger than those of outer cells (B_1 and B_4 in Fig. 4, and B_n in Fig. 5) due to current superposition; the upper and lower current paths in Fig. 5(a), for example, contain B_m–B_n and B_m, respectively. Consequently, larger ac currents tend to flow through inner cells. The larger the number of cells connected in series, the larger will be the ac current flowing through inner cells. Practically, since the ac currents mainly flow through smoothing capacitors, smoothing capacitors with large current rating may be necessary for inner cells when the number of series connection is large.

The operational symmetry of the voltage multiplier explained in the previous subsection allows the assumption of $V_{S\text{-}E} = V_{S\text{-}O} = V_S$. Voltage variation of C_i, ΔV_{Ci}, is yielded from (1) and (2);

$$\Delta V_{Ci} = V_{Ci-O} - V_{Ci-E} = 2V_S - V_i - 2V_D - \frac{2\pi}{\theta} I_{Ci}\left(r_i + r_D\right). \quad (3)$$

In general, the voltage variation of a capacitor can be expressed using an equivalent resistance R_{eq};

$$\Delta V = \frac{It}{C} = \frac{I}{Cf} = IR_{eq}. \quad (4)$$

Substitution of (4) into (3) produces

$$2V_S = V_i + 2V_D + \frac{I_{Ci}}{2} R_{eq-i}, \quad (5)$$

where $R_{eq\text{-}i}$ is the equivalent resistance given by

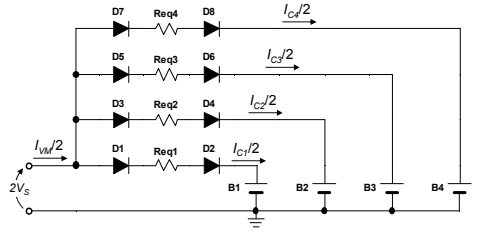


Fig. 6. DC equivalent circuit of voltage multiplier for four cells.

$$R_{eq-i} = 2\left\{\frac{1}{C_i f} + \frac{2\pi}{\theta}\left(r_i + r_D\right)\right\}. \quad (6)$$

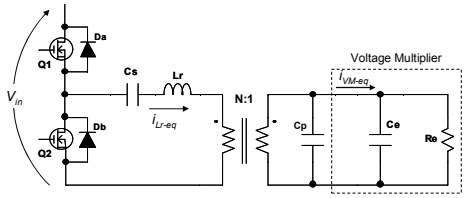
A dc equivalent circuit of the voltage multiplier in the proposed equalizer is derived from (5) as shown in Fig. 6, which is for four cells, B_1–B_4. I_{VM} is equal to the sum of I_{C1}–I_{C4}. The input voltage for the voltage multiplier in the original circuit shown in Fig. 5 is V_S (= $V_{S\text{-}E}$ = $V_{S\text{-}O}$), while that in the derived equivalent circuit shown in Fig. 6 is doubled to $2V_S$ as (5) indicates. Therefore, the input current in the equivalent circuit is halved to $I_{VM}/2$. This derived equivalent circuit resembles that in the conventional equalizer [36], but the value of $R_{eq\text{-}i}$ differs because of the conduction angle of θ; (6) implies that the smaller the conduction angle of θ, the larger the equivalent resistance of $R_{eq\text{-}i}$. Since each cell is connected to the common terminal through each equivalent resistor and two diodes, the current of $I_{VM}/2$ is preferentially distributed to a cell having the lowest voltage. As the power distribution progresses, voltages of cells with low initial voltages increase, whereupon all cell voltages become balanced. Equation (6) implies that mismatching in C_i and r_i results in nonuniform $R_{eq\text{-}i}$ that may eventually cause voltage imbalance in the form of $I_{Ci}R_{eq\text{-}i}/2$. To mitigate the parameter mismatching issue, $I_{Ci}R_{eq\text{-}i}/2$ should be designed low enough compared with V_i. Detail is discussed in Section IV-B,

In this subsection, the voltage multiplier was analyzed by assuming that impedances of smoothing capacitors are negligibly small. However, if not sufficiently small, an impedance of each current path, shown in Fig. 5, would be nonuniformly affected depending on the number of cells contained in each current path, resulting in nonuniform values of $R_{eq\text{-}i}$ for each current path. Therefore, low impedance capacitors, such as low ESR ceramic capacitors, are recommended for smoothing capacitors so that $R_{eq\text{-}i}$ for each current path can be uniform. As long as impedances of smoothing capacitors are negligibly small, equations developed in this subsection are ensured.

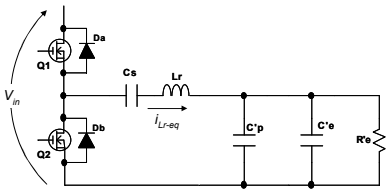
C. Modeling for Parallel-Resonant and Series-Parallel-Resonant Inverters

As aforementioned, the operation of the proposed equalizer resembles that of a PRI/SPRI with a capacitive output filter. In the analysis made in [37],[40], a full-bridge rectifier and capacitive filter load are approximately represented by a resistive-capacitive (R_e–C_e) equivalent circuit.

Since the average power supplied to the voltage multiplier is $(V_i/2+V_D)I_{VM}$ (see Fig. 3), an equivalent resistance of the voltage multiplier, R_{VM}, can be approximated as



(a) Equivalent circuit with a transformer.



(b) Equivalent circuit without a transformer.

Fig. 7. Equivalent circuit for PRI/SPRI with a voltage multiplier.

$$R_{VM} = \frac{\frac{V_i}{2} + V_D}{I_{VM}}. \tag{7}$$

The PRI/SPRI with the voltage multiplier in the proposed equalizer can be approximated similarly to [37], as shown in Fig. 7(a). In [37], the major parameters for the equivalent circuit are yielded as listed below:

$$\theta = 2\,arctan\sqrt{\frac{\pi}{2}\frac{1}{\omega C_p R_{VM}}}, \tag{8}$$

$$k_v = 1 + 0.27\,sin\left(\frac{\theta}{2}\right), \tag{9}$$

$$\beta = -25\,sin\,\theta\,[deg], \tag{10}$$

$$R_e = \frac{R_{VM} k_v^{\,2}}{2}, \tag{11}$$

$$C_e = \frac{2}{\omega R_{VM} k_v^{\,2}} tan|\beta|, \tag{12}$$

where k_v is the voltage waveform coefficient, β is the phase angle between the first harmonics of the primary transformer voltage and current (Fig. 8), and R_e and C_e are the equivalent resistance and capacitance, respectively. The theoretical operation waveforms of the original circuit shown in Fig. 2 and the equivalent circuit shown in Fig. 7(a) are compared in Fig. 8. The waveforms of i_{VM} and v_{Cp} in the original circuit include high harmonics, especially in i_{VM}, whereas those of the equivalent circuit are almost approximated to sinusoidal waves, considerably facilitating analysis. Meanwhile, the waveforms of i_{Lr} and i_{Sa} in the original and equivalent circuits are almost identical (not compared in Fig. 8), indicating that the characteristic of the original circuit is properly approximated by the equivalent circuit. By eliminating the transformer, Fig. 7(a) can be redrawn as shown in Fig. 7(b), in which the values of C'_p, C'_e, and R'_e are

$$C'_p = \frac{C_p}{N^2}, \quad C'_e = \frac{C_e}{N^2}, \quad R'_e = N^2 R_e. \tag{13}$$

The impedance of the equivalent circuit shown in Fig. 7(b) is

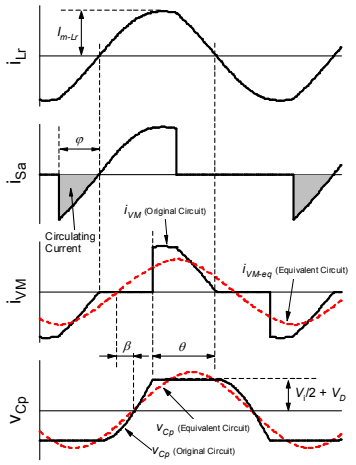


Fig. 8. Waveforms of the original circuit (Fig. 2) and equivalent circuit (Fig. 7(a)).

expressed as

$$Z = \frac{R'_e\left[\left(1 + A + \frac{C'_e}{C}\right)\left\{\frac{A}{1+A} - \left(\frac{\omega}{\omega_0}\right)^2\right\} + 1\right] + jZ_0\left[\left(\frac{\omega}{\omega_0}\right) - \left(\frac{\omega_0}{\omega}\right)\frac{A}{1+A}\right]}{1 + j\frac{R'_e}{Z_0}\left(\frac{\omega}{\omega_0}\right)\left(1 + A + \frac{C'_e}{C}\right)}, \tag{14}$$

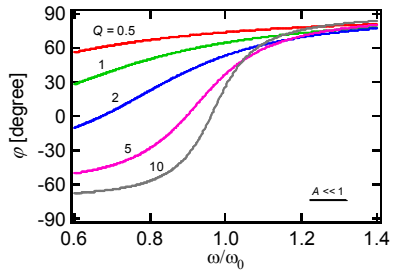
where C and A are defined as

$$C = \frac{C_s C'_p}{C_s + C'_p}, \quad A = \frac{C'_p}{C_s}, \tag{15}$$

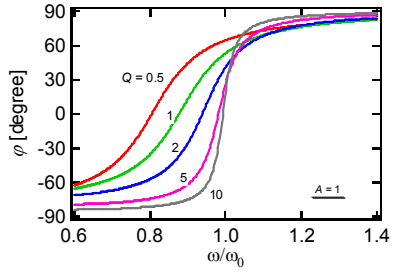
and ω_0 is the characteristic angular frequency, and Z_0 is the characteristic impedance of the resonant inverter;

$$\omega_0 = \frac{1}{\sqrt{L_r C}}, \quad Z_0 = \omega_0 L_r = \frac{1}{\omega_0 C} = \sqrt{\frac{L_r}{C}}. \tag{16}$$

If C_s and C'_p are comparable, the circuit operates as an SPRI (A = 1 is the most common for SPRIs). Meanwhile, if A << 1,

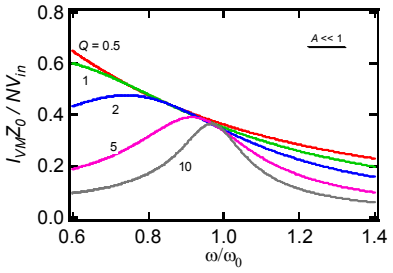


(a) PRI (A << 1).

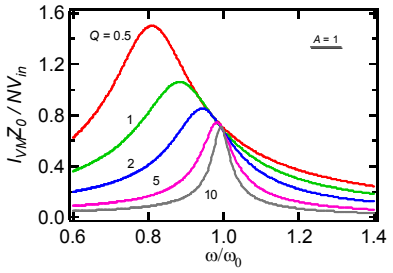


(b) SPRI (A = 1).

Fig. 9. φ as a function of normalized frequency of ω/ω_0.

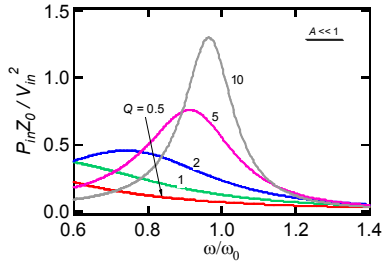


(a) PRI (A << 1).

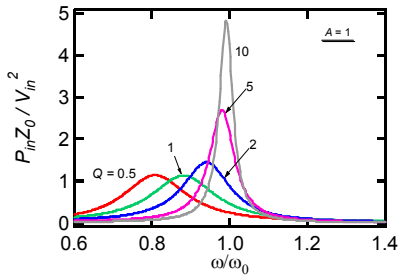


(b) SPRI (A = 1).

Fig. 10. Normalized I_{VM} as a function of normalized frequency of ω/ω_0.



(a) PRI (A << 1).



(b) SPRI (A = 1).

Fig. 11. Normalized P_{in} as a function of normalized frequency of ω/ω_0.

which means that C_s acts as a dc blocking capacitor, the characteristic of a PRI is obtained. By arranging (14),

$$|Z| = \sqrt{\frac{R'^{2}_{e}\left[\left(1+A+\frac{C'_e}{C}\right)\left\{\frac{A}{1+A}-\left(\frac{\omega}{\omega_0}\right)^2\right\}+1\right]^2+Z_0^2\left[\left(\frac{\omega}{\omega_0}\right)-\left(\frac{\omega_0}{\omega}\right)\frac{A}{1+A}\right]^2}{1+\left(\frac{R'_e}{Z_0}\right)^2\left(\frac{\omega}{\omega_0}\right)^2\left(1+A+\frac{C'_e}{C}\right)^2}} \quad . \quad (17)$$

The amplitude of i_{Lr}, $I_{m\text{-}Lr}$, is obtained from (17) and Fourier series, as

$$I_{m-Lr} = \frac{2V_{in}}{\pi|Z|}, \quad (18)$$

where V_{in} is the input voltage of the PRI/SPRI, which is equal to the sum of cell voltages in the practical circuit. Equation (14) can be rearranged to

$$Z = \frac{R'_e + j\left[Z_0\left\{\left(\frac{\omega}{\omega_0}\right)-\left(\frac{\omega_0}{\omega}\right)\frac{A}{1+A}\right\}-\frac{R'^{2}_{e}}{Z_0}\left(\frac{\omega}{\omega_0}\right)\left(1+A+\frac{C'_e}{C}\right)\left\{\left(1+A+\frac{C'_e}{C}\right)\left(\frac{A}{1+A}-\left(\frac{\omega}{\omega_0}\right)^2\right)+1\right\}\right]}{1-\left[\frac{R'_e}{Z_0}\left(\frac{\omega}{\omega_0}\right)\left(1+A+\frac{C'_e}{C}\right)\right]^2} \quad . \quad (19)$$

From (19), the phase lag, φ, is expressed as

$$\varphi = \arctan\left[\frac{Z_0}{R'_e}\left\{\left(\frac{\omega}{\omega_0}\right)-\left(\frac{\omega_0}{\omega}\right)\frac{A}{1+A}\right\}-\frac{R'_e}{Z_0}\left(\frac{\omega}{\omega_0}\right)\left(1+A+\frac{C'_e}{C}\right)\left\{\left(1+A+\frac{C'_e}{C}\right)\left(\frac{A}{1+A}-\left(\frac{\omega}{\omega_0}\right)^2\right)+1\right\}\right] \quad . \quad (20)$$

φ as a function of normalized frequency of ω/ω_0 for the PRI and SPRI are shown in Figs. 9(a) and (b), respectively. From the integral of i_{Lr} and (20), the average input current of the PRI/SPRI, $I_{in\text{-}ave}$, which is equal to that of i_{Sa}, is obtained as

$$\begin{aligned} I_{in-ave} &= \frac{1}{2\pi}\int_0^{\pi} i_{Lr}\,d\omega t = \frac{I_{m-Lr}}{2\pi}\int_0^{\pi} sin(\omega t-\varphi)d\omega t \\ &= \frac{2V_{in}\cos\varphi}{\pi^2|Z|} \end{aligned} \quad . \quad (21)$$

The average current of i_{VM} over a half the switching period, I_{VM}, is yielded as follows:

$$\begin{aligned} I_{VM} &= \frac{1}{\pi}\int_{\varphi+\pi-\theta}^{\varphi+\pi} Ni_{Lr}\,d\omega t = \frac{NI_{m-Lr}}{\pi}\int_{\varphi+\pi-\theta}^{\varphi+\pi} sin(\omega t-\varphi)d\omega t \\ &= \frac{2NV_{in}}{\pi^2|Z|}(1-\cos\theta) \\ &= NI_P \end{aligned} \quad . \quad (22)$$

The normalized I_{VM} , I^*_{VM}, is defined as

$$I^*_{VM} = I_{VM}\frac{Z_0}{NV_{in}} . \quad (23)$$

I^*_{VM} as a function of normalized frequency, ω/ω_0, for the PRI (A << 1) and SPRI (A = 1) are shown in Figs. 10(a) and (b). Here, the quality factor Q is defined as

$$Q = \frac{N^2R_{VM}}{Z_0} . \quad (24)$$

It emerges that I^*_{VM} at ω/ω_0 = 1 is almost constant, although it declines slightly with increasing Q. These characteristics indicate that currents supplied from the PRI/SPRI to the voltage multiplier are almost constant at ω/ω_0 = 1, even for cells with 0 V (i.e. V_i = 0 V or R_{VM} = 0 based on (7)). Accordingly, currents in the proposed equalizer can be inherently limited under desired levels, and the equalizer can operate safely, even when some cell is 0 V.

I^*_{VM} of the SPRI at ω/ω_0 = 1 is approximately twice as large as that of the PRI, which implies that at a given Z_0, the SPRI produces almost twice the I_{VM} than the PRI. In other words, for a given I_{VM}, the Z_0 of the PRI can be halved compared to that of the SPRI. This means that, for a given I_{VM}, C and L_r in the PRI are larger and smaller, respectively (see (16)), than in the SPRI. In general, inductors are one of the bulkiest components, which occupy considerable space and footprint within a circuit, and their reduced inductance contributes to the inductor compactness. Since L_r in the PRI can be designed smaller than in the SPRI, the PRI is considered advantageous over the SPRI in terms of circuit miniaturization.

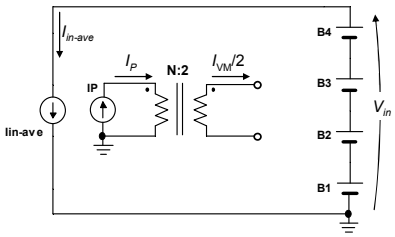


Fig. 12. DC equivalent circuit for PRI/SPRI.

The input power for the equalizer, $P_{in} = V_{in} \times I_{in\text{-}ave}$, is dependent of φ and $|Z|$, according to (21). The normalized P_{in}, P^*_{in}, is defined as

$$P^*_{in} = P_{in}\frac{Z_0}{V_{in}^2} = \frac{2Z_0 \cos\varphi}{\pi^2|Z|}. \quad (25)$$

P^*_{in} as a function of normalized frequency of ω/ω_0 for the PRI and SPRI are shown in Figs. 11(a) and (b), respectively. In conventional PRIs/SPRIs, N is a parameter crucial to determine a voltage conversion ratio. In the proposed equalizers, on the other hand, since both the input and output of equalizers are a voltage source, the voltage conversion ratio is no longer a controllable parameter. Therefore, N in the proposed equalizer can be used as a design freedom. Detailed design guide is discussed in Section IV.

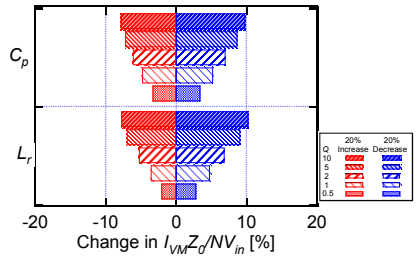
From (21) and (22), a dc equivalent circuit for the PRI/SPRI can be derived as shown in Fig. 12. For consistency with the equivalent circuit for the voltage multiplier that is supposed to receive the current of $I_{VM}/2$, as shown in Fig. 6, the transformer turn ratio in Fig. 12 is modified to N:2 to supply the current of $I_{VM}/2$. The series connection of B_1–B_4 supplies a current of $I_{in\text{-}ave}$ to the input of the PRI/SPRI. A current of I_P is generated and fed to the transformer primary winding, whereupon the current is converted to $I_{VM}/2$ on the secondary side.

D. Sensitivity Analysis for Constant Current Characteristic

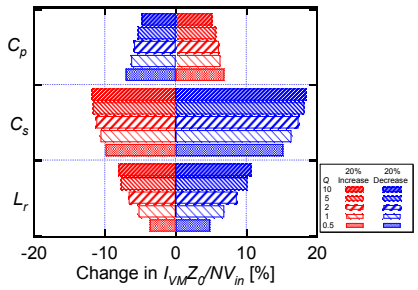
The constant current characteristic of the normalized I_{VM} at $\omega/\omega_0 = 1$ shown in Fig. 10 implies that the proposed equalizers can operate safely even at a fixed frequency, hence simplifying the circuitry by eliminating feedback control loop. However, for the equalizers to operate without feedback control, the influence of parameter changes due to such as component tolerance, temperature, and aging on the constant current characteristic should be took into consideration.

The sensitivity analysis was performed to investigate the percentage impact of each component parameter on the constant current characteristic. Parameters in the voltage multiplier were excluded from the sensitivity analysis because, in the analysis performed in the previous subsection, the voltage multiplier was expressed as R_{VM} (see (7)) that is then reflected in Q (see (24)), and the influences of changes in Q on the constant current characteristics are shown in Fig. 10. Therefore, parameters in the PRI/SPRI (C_p, C_s, and L_r) were considered for the sensitivity analysis. The percentage impacts of ±20% change in each parameter on the normalized I_{VM} were investigated.

The results of the sensitivity analysis performed for the PRI



(a) PRI ($A << 1$).



(b) SPRI ($A = 1$).

Fig. 13. Percentage impact of ±20% change in C_p, C_s, and L_r on normalized I_{VM} at ω/ω_0.

($A << 1$) and SPRI ($A = 1$) are shown in Figs. 13(a) and (b), in which the percentage impacts on the normalized I_{VM} at $\omega/\omega_0 = 1$ are illustrated in the form of a tornado diagram. For example, if C_p at $Q = 10$ in the PRI increased (decreased) by 20%, the normalized I_{VM} would decrease (increase) by approximately 7.8% (9.8%). The impact of change in C_s in the PRI was infinitesimal and is not shown in Fig. 13(a) because C_s in the PRI acts as a dc blocking capacitor, which generally has a negligible impact on PRI's characteristics as long as its capacitance C_s is large enough compared to C_p. Except for C_p in the SPRI, the impacts of parameter changes became insignificant as Q decreased, implying that the constant current characteristics would be insusceptible to parameter changes at low Q values. The change in C_s in the SPRI showed relatively large impacts, while impacts of C_p and L_r in both the PRI and SPRI were almost less than 10%.

Changes in the normalized I_{VM} are allowable to some extent in the proposed equalizers because the constant current characteristic at $\omega/\omega_0 = 1$ is not a strict requirement; the constant current characteristic serves as inherent current limitation, and the equalizers can operate safely as long as currents are limited under desired current levels. However, the sensitivity analysis performed here is considered important to ensure that changes in the normalized current never go beyond allowable boundaries.

E. Derivation of DC Equivalent Circuit

By combining the derived equivalent circuits for the voltage multiplier and the PRI/SPRI shown in Figs. 6 and 12, respectively, a dc equivalent circuit for the proposed equalizer can be yielded as shown in Fig. 14, in which an ideal multi-winding transformer with a turn ratio of N:2:2:2:2 is used for cells to be connected in series. Although this dc equivalent

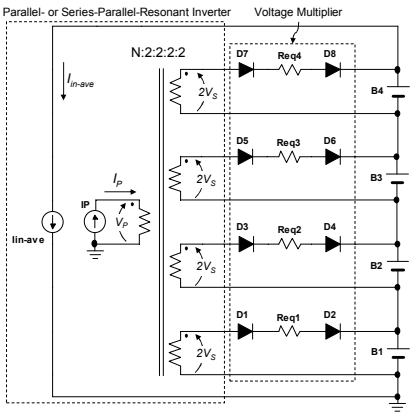


Fig. 14. DC equivalent circuit for the proposed equalizer for four cells connected in series.

circuit also resembles that derived in [36], equations for $R_{eq\text{-}i}$, $I_{in\text{-}ave}$, and I_P, which are given by (6), (21), and (22), respectively, are totally different.

The derived dc equivalent circuit provides an intuitive understanding of how cell voltages are equalized in the proposed equalizer. The series-connected cells of B_1–B_4 power the PRI/SPRI, whereupon the provided power is transferred to the voltage multiplier through the ideal multi-winding transformer. The transferred power is then preferentially redistributed to a cell having the lowest voltage. The voltage of this cell thus increases due to power received from the voltage multiplier, whereas those of other cells decrease by supplying power to the PRI/SPRI. As the power redistribution progresses, all the cell voltages ultimately become uniform.

F. Determination for Capacitance of C_p, C_s, and C_i

For the PRI/SPRI to operate properly, C_i in the voltage multiplier should be designed to not influence the resonant operation. According to the derived dc equivalent circuit shown in Fig. 6 and (6), a dc current flowing through $R_{eq\text{-}i}$ in the equivalent circuit represents an ac current flowing through C_i in the original circuit. When cell voltages of B_1–B_4 in Fig. 6 (or Fig. 14) are balanced, the current from the PRI/SPRI is uniformly distributed to B_1–B_4 through a respective equivalent resistor, meaning the current from the PRI/SPRI in the original circuit is distributed to all of C_1–C_4, as shown in Fig. 4. Conversely, current concentration to one of the equivalent resistors is likely when cell voltages are imbalanced, since the current preferentially flows toward a cell having the lowest voltage, as explained in Section III-B. This means that only one of C_1–C_4 in the original circuit is in the current flow path when cell voltages are not balanced. Considering the current flow path under the voltage-imbalanced condition, C_i should be designed to be sufficiently larger than C_p as well as N^2C_s, which is the reflected capacitance of C_s on the secondary side, so that C_i does not influence the resonant operation. Thus, from (13) and (15), C_i should satisfy

$$C_i >> C_p = AN^2C_s . \quad (26)$$

IV. Design Guide

In this section, an equalizer using a PRI is designed for 12 cells connected in series as an example, but similar development can be made for equalizers using a SPRI. The target design is as follows: V_i = 0–4.0 V that covers voltage variation ranges of EDLCs (0–3.0 V) and LICs (2.0–4.0 V), 10 W at a maximum V_{in} = 48 V (4.0 V/cell × 12 cells), and $f_0 = \omega_0/2\pi < 200$ kHz. A voltage multiplier is assumed to consist of capacitors (C_i = 47 μF, r_i = 80 mΩ) and diodes (V_D = 0.45 V, r_D = 35 mΩ). Component values determined in this section will be used for simulation analysis and a prototype for the experiment.

A. Parallel-Resonant Inverter

According to Fig. 6, $I_{VM}/2$ is the sum of $I_{Ci}/2$ (i = 1…12), which corresponds to a current flowing toward B_i. Under a voltage-balanced condition,

$$\frac{I_{VM}}{2} = \frac{I_{C1}}{2} + \ldots + \frac{I_{C12}}{2} = 12 \times \frac{10[W]}{12[cells] \times 4.0[V]} = 2.5[A]. \quad (27)$$

From (7) and (27),

$$R_{VM} = \frac{V_i/2 + 0.45[V]}{5[A]} = 0.09 \sim 0.49[\Omega]. \quad (28)$$

Although (27) is for the voltage-balanced condition, an identical value of R_{VM} is obtained for voltage-imbalanced conditions.

As shown in Fig. 9(a), as Q decreases, φ at $\omega/\omega_0 = 1$ increases. Meanwhile, circulating current, which corresponds to the filled area in Fig. 8, becomes large with φ, increasing conduction losses in the switches and anti-parallel diodes. Hence, Q should be designed high to reduce the losses. By substituting (13), (15), and (16) into (24), Q can be rewritten as

$$Q = \omega_0 R_{VM} C_p . \quad (29)$$

A high-Q design could be feasible with large C_p, but (26) needs to be satisfied. Given a frequency limit of $f_0 < 200$ kHz and (26) with C_i = 47 μF, $Q \approx 1.0$ ($\varphi \approx 60°$) at V_i = 4.0 V (R_{VM} = 0.49 Ω) was concluded to be a reasonable design target. C_p = 1.92 μF was used as a practical design value.

According to Fig. 11(a) or (25), the value of Z_0 at $Q \approx 1$ needs to be about 30 Ω. From (13), (15), and (16), L_r, N, and f_0 were determined to be 25 μH, 8, and 183.7 kHz, respectively, with which Z_0 is 28.85 Ω at Q = 1.09.

B. Voltage Multiplier

As mentioned in Section III-B, parameter mismatching may cause voltage imbalance. In this subsection, a design of a voltage multiplier consisting of capacitors (C_i = 47 μF, r_i = 80 mΩ) and diodes (V_D = 0.45 V, r_D = 35 mΩ) is verified for a target voltage imbalance of 40 mV, which is 1/100 of V_i = 4.0 V, with considering component tolerance.

At V_i = 4.0 V (R_{VM} = 0.49 Ω and θ = 100.5° (see (8)), $R_{eq\text{-}i}$ is 1.06 Ω according to (6). Since $R_{eq\text{-}i}$ contains several parameters, tolerance for $R_{eq\text{-}i}$, not for each component parameter, was considered for the sake of simplicity. As discussed in the previous subsection, a current flowing toward each cell is $I_{Ci}/2$ that is 0.208 A under a voltage-balanced condition. Therefore, if tolerance for $R_{eq\text{-}i}$ is 20%, the voltage imbalance, $V_{imbalance}$, is estimated to be

$$V_{imbalance} = 0.208[A] \times 1.06[\Omega] \times 20\% = 44mV \approx 40mV \,. \quad (30)$$

Thus, the target voltage imbalance is almost satisfied for 20% tolerance for $R_{eq\text{-}i}$. This equation means that the lower the current, the smaller will be the possible voltage imbalance, and vice versa. Hence, the voltage multiplier should be designed considering equalization current as well as component tolerance so that possible voltage imbalance is within allowable range.

V. Simulation Analysis

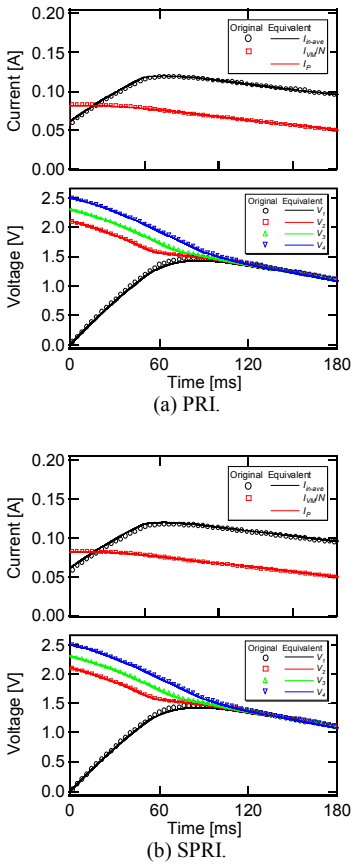
To verify the dc equivalent circuit derived in Section III-E, the equalization characteristics of the original and dc equivalent circuits, shown in Figs. 2 and 14, respectively, were compared based on simulation analyses. Simulation-based equalization tests were performed for both PRI- and SPRI-based equalizers for four cells connected in series.

The component values determined for the PRI-based equalizer for 12 cells in the previous section were used, although the number of series connection for the simulation analysis was 4. As discussed in Section III-C, for a given I_{VM}, Z_0 of the PRI can be reduced to almost half that of the SPRI. The SPRI for the simulation was designed so that I_{VM} of the SPRI was the same as that of the PRI. Component values for the PRI (SPRI) were C_s = 1 μF (30 nF), C_p = 1.92 μF (1.92 μF), L_r = 25 μH (50 μH), and N_1:N_2 = 8:1 (8:1). Ideal switches were used for Q_a and Q_b, and operated with a duty cycle of 50% at a fixed switching frequency of 183.7 kHz. Parameters used for the voltage multiplier in the original circuit were C_i = 47 μF, r_i = 80 mΩ, r_D = 35 mΩ, and V_D = 0.45 V. $R_{eq\text{-}i}$, $I_{in\text{-}ave}$, and I_P in the dc equivalent circuit were programmed to obey (6), (21), and (22), respectively. Capacitors with a capacitance of 10 mF were used for Bi, and simulation-based equalization tests were performed from an initially-voltage-imbalanced condition; V_1–V_4 were 0, 2.1, 2.3, and 2.5 V.

The simulation results of the original and dc equivalent circuits are compared in Fig. 15. The voltages of cells with high initial voltages decreased by supplying power to the equalizer, while V_1, which was the lowest initial voltage, increased by receiving power from the equalizer. The voltage imbalance was gradually reduced over time and almost eliminated at approximately 120 ms. Thanks to the inherent constant current characteristic discussed in Section III-C, no excessive current flowed, even when V_1 was 0 V at the beginning of the simulation.

Equalization profiles in the original and equivalent circuits for both the PRI- and SPRI-based equalizer correlated well, confirming that the derived dc equivalent circuit properly represents the characteristics of the original circuits. The original circuit-based simulation took hours to complete 33066 switching cycles (183.7 kHz × 180 ms), whereas the equivalent circuit simulation was completed in an instant due to the lack of high-frequency switching devices. The equivalent circuit thus saves considerable simulation time and burden, and can be a useful tool in determining equalization characteristics under a given condition.

The simulation results of PRI- and SPRI-based equalizers



(a) PRI.

(b) SPRI.

Fig. 15. Simulation results of original and derived dc equivalent circuits for equalizers using (a) PRI and (b) SPRI.

were almost identical, proving that Z_0 as well as L_r of the PRI can be halved compared to that of the SPRI to achieve the same equalization performance. Since virtually identical performance can be achieved with a reduced L_r in the PRI-based equalizer, the following experimental section shows the results of the PRI-based equalizer only to save page length.

VI. Experimental Results

A. Prototype and Experimental Setup

A 10-W prototype of the proposed equalizer using a PRI designed in Section IV was built for 12 cells connected in series, as shown in Fig. 16. The component values are listed in Table I. With ceramic capacitors for C_1–C_{12}, the prototype could had been designed even more compactly, but their voltage-dependent capacitance was considered unsuitable; nonuniform capacitance results in nonuniform $R_{eq\text{-}i}$ (see (6)) and may consequently cause voltage imbalance, as discussed in Sections III-B and IV-B. Therefore, tantalum capacitors, whose capacitance is not dependent on applied voltage, were used for C_1–C_{12} to make each capacitance uniform as well as $R_{eq\text{-}i}$. MOSFETs were driven by a boot-strap gate driver IC (UCC27200, Texas Instruments) at a fixed frequency of 183.7 kHz with a duty cycle of 47%. Low ESR ceramic capacitors were used for C_{out1}–C_{out12} so that the equalization performance of the voltage multiplier is not adversely affected, as discussed

Table I. Component values.

	Component	Value
Voltage Multiplier	C_1–C_{12}	Tantalum Capacitor, 47 µF, 80 mΩ
	C_{out1}–C_{out12}	Ceramic Capacitor, 200 µF, 1.5 mΩ
	D_1–D_{24}	Schottky Diode, DFLS220L-7, V_D = 0.45 V, r_D = 35 mΩ
Parallel-Resonant Inverter	C_s	Film Capacitor, 1 µF
	C_p	Film Capacitor, 1.92 µF
	L_r	22 µH
	Transformer	N_1 :N_2 = 16:2, L_{lg} = 3.0 µH, L_{mg} = 482 µH
	Q_a, Q_b	N-Ch MOSFET, HAT2266H, R_{on} = 9.2 mΩ
	D_a, D_b	Schottky Diode, 30BQ060PbF, V_D = 0.52 V

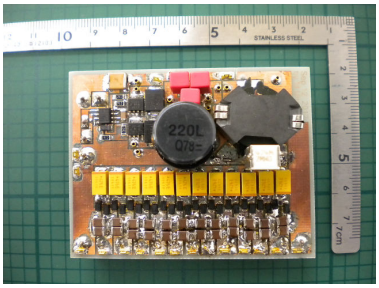


Fig. 16. A 10-W prototype of an equalizer using PRI for 12 cells connected in series.

in Section III-B. Inherent body diodes of MOSFETs could had been used as anti-parallel diodes of D_a and D_b, which conduct during dead time periods. However, inherent body diodes are typically inferior in terms of the forward voltage drop of V_D to external Schottky diodes, hence increasing diode losses. External Schottky diodes were placed in parallel with the MOSFETs to bypass the inherent body diodes and prevent these from affecting the equalizer's efficiency.

An experimental setup for the power conversion efficiency measurement is illustrated in Fig. 17. The equalizer was powered by an external power source, V_{ext}, while cells were removed and a variable resistor was connected to either terminal X or Y to emulate voltage-imbalanced or -balanced conditions, respectively. The current flow paths under a voltage-imbalanced condition, where B_1 has the lowest voltage among B_1–B_{12}, can be emulated when X is selected. Conversely,

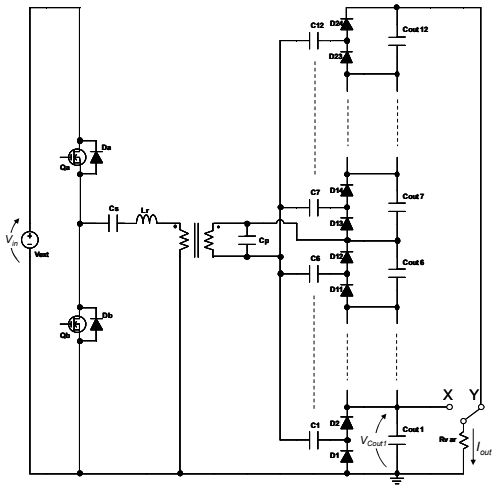
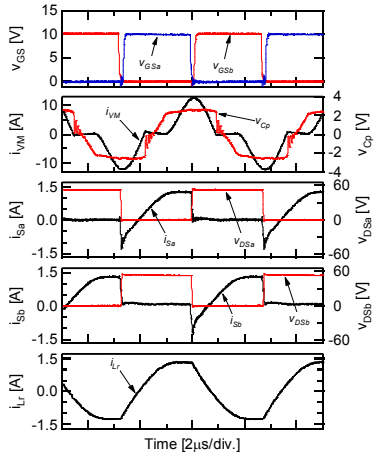


Fig. 17. Experimental setup for power conversion efficiency measurement.

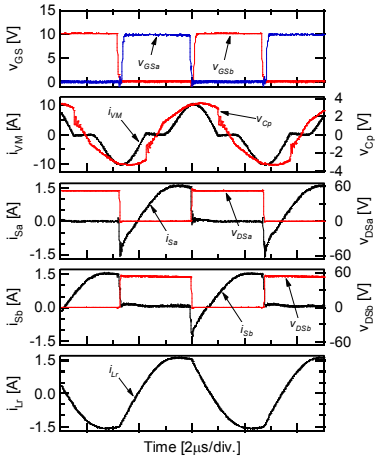
selecting Y emulates the current flows under a voltage-balance condition, which resembles those in Fig. 4. To cover the voltage variation range of EDLCs and LICs whose voltage ranges are about 0–3.0 V and 2.0–4.0 V, respectively, the input voltage for the equalizer, V_{in}, was varied up to 48 V, which corresponds to a total voltage of 12 cells each having ≤ 4.0 V/cell, and the power conversion efficiency was measured by varying the ratio of V_{Cout1} to V_{in} (V_{Cout1}/V_{in}) between 0 and 1/12; V_{Cout1} is the voltage of C_{out1}.

B. *Measured Waveforms and Power Conversion Efficiencies*

Measured waveforms at V_{in} = 48 V and V_{Cout1} = 4.0 V under voltage-balanced and -imbalanced conditions are shown in Figs. 18(a) and (b), respectively. Although i_{VM} is supposed to sharply increase as v_{Cp} is clamped under an ideal condition, as shown in Fig. 3, a parasitic inductance in the prototype suppressed the sharp increase and i_{VM} in the experiments changed almost sinusoidally while v_{Cp} was clamped. Oscillation in v_{Cp} during non-clamping periods is also attributed to the parasitic inductance. v_{Cp} during the clamping periods under the voltage-balanced condition was almost constant, although changing slightly due to charging/discharging of C_i. Under the voltage-imbalanced condition, conversely, it changed with i_{VM}

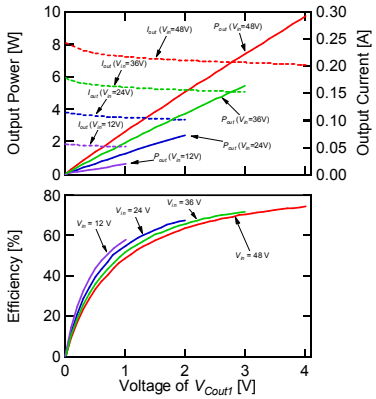


(a) Under voltage-balanced condition.

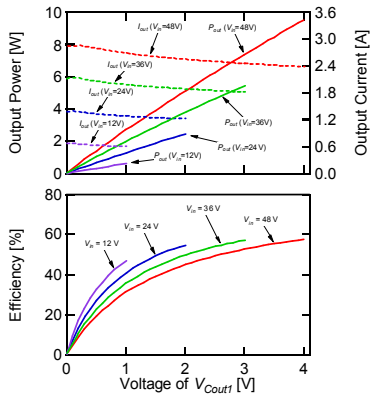


(b) Under voltage-imbalanced condition.

Fig. 18. Measured waveforms at V_{in} = 48 V and V_{Cout1} = 4.0 V.



(a) Under voltage-balanced condition.



(b) Under voltage-imbalanced condition.

Fig. 19. Measured power conversion efficiency, output power, and output current characteristics.

because of the current concentration. Under the voltage-balanced condition, i_{VM} was distributed to each C_i as shown in Fig. 4, whereas that under the voltage-imbalanced condition was concentrated to C_1, resulting in a significant voltage variation due to r_1 (ESR of C_1) as well as charging/discharging of C_1. Accordingly, although not significantly, the characteristic of the PRI was slightly affected based on whether voltages were balanced.

Measured power conversion efficiencies, output powers, and output currents as a function of V_{Cout1} under voltage-balanced and -imbalanced conditions are shown in Figs. 19(a) and (b), respectively. The measured output currents were almost constant and independent on V_{Cout1}, as discussed in Section III-C, demonstrating the constant current characteristic of the proposed equalizer. The power conversion efficiencies consistently increased with V_{Cout1}, while the peak efficiencies under voltage-balanced and -imbalanced conditions were 58–74.2% and 46.6–57.4%, respectively. The inferior efficiencies under the voltage-imbalanced condition can be attributed to the current concentration causing an increased Joule loss. As mentioned above, i_{VM} under the voltage-imbalanced condition concentrated to C_1, and the current concentration caused an increased Joule loss in the form of $i_{VM}^2 r_1$.

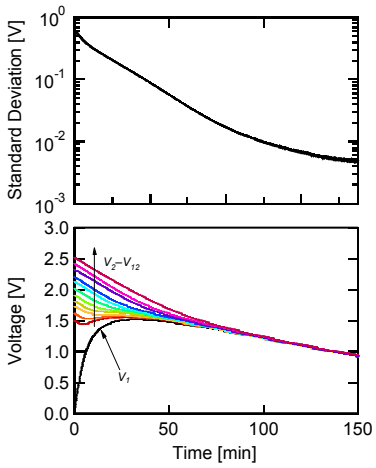


Fig. 20. Experimental equalization profiles of series-connected EDLCs.

C. Equalization for Series-Connected EDLCs

An experimental equalization test was performed for 12 EDLCs, each having capacitance of 500 F at a rated charge voltage of 2.5 V, from a voltage-imbalanced condition where V_1 was 0 V while others were 1.5–2.5 V. Cell voltages were recoded using a data logger (NR-HA08, KEYENCE) with the least significant bit resolution of 0.31 mV.

The resultant equalization profiles are shown in Fig. 20. Similar to the simulation results shown in Fig. 15, V_1 increased by receiving power from the equalizer while others decreased by providing power to the equalizer. The voltage imbalance was gradually eliminated as the power distribution progressed and over time. The standard deviation of cell voltages declined to approximately 5 mV at the end of the equalization test, thus demonstrating the equalization performance of the proposed equalizer.

The cell voltages continued to gradually decrease even after the voltage imbalance was almost eliminated. This gradual decrease in the cell voltages was due to the power conversion loss of the equalizer. Because of the power conversion loss, the power redistributed to the cells from the equalizer was smaller than that supplied to the equalizer from the cells. In other words, the equalizer continued to circulate energies of cells meaninglessly after cell voltages were well-equalized. In general, power requirement for equalizers is considerably smaller than that for SCs and batteries. In [10],[41], for example, a current of C/100 rate is considered appropriate for equalization, and therefore, the loss in the equalizer would be trivial. However, if the loss in the equalizer needs to be minimized, the equalizer should be disable when cell voltages are balanced. To enable/disable equalization depending on voltage conditions, a management system and voltage sensing for each cell would be necessary.

VII. Comparison with Conventional Equalizers

In Table II, where n is the number of cells connected in series, conventional equalizers are roughly categorized into several groups and are compared to the proposed equalizer using a

PRI/SPRI in terms of component count. Equalizers using buck-boost converters [4]–[8] or switched capacitor converters [9]–[17] can be constituted with reasonable component count, but energy transfer of these equalizers is limited between two adjacent cells only (i.e., adjacent cell-to-cell equalization), resulting in relatively slow equalization speed and poor equalization efficiency especially when the number of series connection is large [31],[32]. In other words, energy has to traverse multiple cells, switches, and capacitors/inductors before reaching a target cell [32]. Especially, equalization speed of switched capacitor-based equalizers tends to be slow when a voltage difference between adjacent two cells (ΔV) is small because the switched capacitor equalizers equivalently represent resistive characteristics and its equalization current is qualitatively expressed as $I = \Delta V/R$ [18],[32]. Although equalizers using transformers [18],[19] can reduce the number of inductors, capacitors, and diodes, the size is prone to be bulky because multiple transformers are necessary. Equalizers using a single isolated converter with selection switches [21]–[26] can minimize the number of passive components. Hence, they would be built compact compared to other equalizers, although an intelligent management system as well as multiple switches and/or solid state relays (SSRs) are indispensable to determine and select target cells.

The number of required switches is a good indicator of circuit complexity because each switch requires several auxiliary components including a gate driver, passive components, and/or opto-coupler. Most conventional cell voltage equalizers aforementioned require numerous switches in proportion to the number of series connections [4]–[26], meaning the circuitry of these equalizers is prone to be considerably complex with increasing number of series connections. Conversely, since only two switches are required in the proposed equalizer, the circuit complexity can be dramatically reduced.

The modularity, or extendibility, is also an important index of equalizers so as to be flexibly designed and redesigned. Although equalizers in [27]–[30] need fewer switches, the existence of a multi-winding transformer is considered as a major drawback. The multi-winding transformer impairs modularity due not only to the strict requirement for parameter matching among multiple secondary windings but also the need to change the number of secondary windings. Meanwhile, the proposed equalizer can be constituted with a normal transformer, achieving good modularity. Moreover, the number of series connections can be arbitrarily extended by stacking a capacitor and a diode pair in the voltage multiplier and adjusting the transformer turn ratio.

Magnetic component count has the greatest impact on the size of equalizers. The proposed equalizer needs only two magnetic components (i.e. a transformer and a resonant inductor, L_r), and even a single-magnetic configuration is feasible if the leakage inductance of the transformer is designed to have a proper inductance as L_r. The double- or single-magnetic configuration of the proposed equalizer allows a smaller design compared to conventional equalizers requiring numerous magnetic components [4]–[8],[17]–[19],[33].

Thus, most conventional equalizers have challenges in terms of circuit complexity, modularity, and/or size because of the existence of multiple switches, a multi-winding transformer, and/or multiple magnetic components. The proposed equalizer, on the other hand, consists of two switches, a normal transformer, and a resonant inductor, presumably achieving simplified circuitry, good modularity, and compact design. In addition, unlike the conventional equalizers using buck-boost converters or switched capacitor converters, the proposed equalizer does not suffer from neither slow equalization speed nor poor equalization efficiency because the energy transfer in the proposed equalizer is basically "string-to-cell", not adjacent cell-to-cell, and hence, energy can be directly transferred from the string to a target cell (or the least charged cell) without traversing multiple cells. Besides, since the equalization current in the proposed equalizer is almost constant and independent on cell voltages as mathematically discussed in Section III-C, the equalization speed is essentially constant and independent on cell voltage conditions.

When compared to conventional single- and double-switch equalizers using a voltage multiplier, the proposed equalizer offers some beneficial features. The resonant operation of the

Table II. Comparison between conventional and proposed equalizers in terms of component count.

Topology		Switch	L	C (*)	D	Transformer
Buck-Boost Converter	Basic Topology [4]	$2(n-1)$	$n-1$	-	-	-
	Ćuk Converter [5]	$2(n-1)$	$2(n-1)$	$n-1$	-	-
	[7], [8]	n	$n-1$	-	-	-
Switched Capacitor Converter	Basic Topology [9], [10]	$2n$	-	$n-1$	-	-
	Double-Tiered [11]	$2n$	-	$2n-3$	-	-
	Quasi-Resonant [17]	$2n$	$n-1$	$n-1$	-	-
Converter Using Transformer	Flyback Converter [18], [19]	1 and n SSRs	-	-	n	n
	Multi-Winding Transformer [20]	$2n$	-	-	-	1 with $n/2$ secondaries
Isolated Converter with Selection Switches	[21]	2 and $2n$ SSRs	-	-	2	2
	[22]	$n+1$	-	-	-	1 with n secondaries
	[23]	$2(n+1)$	-	-	$2n-1$	1
	[24]	2 and $2n$ SSRs	-	-	-	1
Multi-Winding Trasformer	Forward Converter [27]–[29]	2	-	-	$n+2$	1 with n secondaries
	Half-Bridge Converter [30]	2	1	2	$4n$	1 with n secondaries
Multi-Stacked Buck-Boost Converter [33]		1	$n+1$	n	n	-
Single-Switch with Voltage Multiplier	Equalizer [34]	1	-	n	$2n$	1
	Charger [35]	1	1	n	$2n$	-
Double-Switch with Voltage Multiplier	Half-Bridge Inverter [36]	2	-	$n+1$	$2n$	1
	PRI/SPRI [Proposed]	2	1	$n+2$	$2n$	1

(* Smoothing capacitor is excluded)

proposed equalizer can dramatically mitigate issues on current stresses and EMI compared to the conventional single-switch equalizer/charger [34],[35], in which high capacitive inrush currents are very likely. Furthermore, the inherent constant current characteristic of the PRI/SPRI, which was mathematically analyzed and experimentally demonstrated in Sections III-C and VI-B, respectively, is a very desirable feature especially for EDLCs, whose voltages vary down to 0 V—EDLCs with 0 V can be regarded as a short-circuit load. The conventional double-switch equalizer [36], for example, may be able to operate with an open-loop control (fixed-duty operation), but a large current is very likely to flow and possibly destroy the circuit when some SC voltage is too low because currents in the equalizer tend to be large as the voltage difference between an equalizer's input and cell expands. In other words, the conventional double-switch equalizer operates as a voltage source for cells. In the proposed equalizer using a PRI/SPRI, conversely, even with an open-loop control (fixed-frequency operation), the current supplied from the PRI/SPRI to the voltage multiplier is limited under a desired level, even when some SC voltage is 0 V, because the proposed equalizer using a PRI/SPRI virtually operates as a constant current source. Hence, in the proposed equalizer, not only the circuitry can be further simplified by eliminating the feedback control loop, but the equalizer can operate safely for SCs at any voltage.

VIII. Conclusions

A double-switch cell voltage equalizer using a PRI/SPRI and voltage multiplier was proposed. The proposed equalizer achieves simplified circuitry as well as good modularity because neither multiple switches nor a multi-winding transformer are necessary. In addition, the inherent constant current characteristic of the PRI/SPRI at a fixed frequency not only eliminate the need for feedback control to limit currents under desired levels but also mean the proposed equalizer can operate safely, even when some cell voltage is 0 V.

Detailed operation analyses were separately performed for the voltage multiplier and PRI/SPRI. Based on mathematical analyses, dc equivalent circuits for the voltage multiplier and PRI/SPRI were derived, whereupon, by combining these equivalent circuits, the dc equivalent circuit for the whole equalizer was obtained. Simulation-based equalization profiles showed good correlation, verifying the derived equivalent circuit.

A 10-W prototype of the proposed equalizer for 12 cells connected in series was built, and an experimental equalization test was performed for series-connected EDLCs from an initially-voltage-imbalanced condition. The voltage imbalance was gradually eliminated by the equalizer, and the standard deviations of cell voltages decreased low enough at the end of the experiments, demonstrating the equalization performance of the proposed equalizer.

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