Highly Extendable Interleaved High Step-Up Boost Converter with Automatic Current Balancing and Reduced Semiconductor Voltage Stresses for Renewable Energy Systems

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Abstract—**Boost converters with a high step-up conversion ratio, and a large input current capability are needed for low-voltage renewable energy resources, such as photovoltaic panels and fuel cells, to be connected to the grid. Interleaved converters consisting of parallel-connected multiple converters are a suitable topology for low-voltage large input current applications. Conventional interleaved converters, however, face a variety of challenges, such as the necessity of additional current control loops to actively balance multiple phase currents, high voltage stresses of semiconductors, insufficient step-up conversion ratios, and poor flexibility to be applied to various renewable energy sources. This paper proposes a highly extendable interleaved high step-up boost converter with an automatic current balancing capability and reduced voltage stresses of semiconductors, thanks to added capacitors. Step-up conversion ratios and input current capacities of the proposed converters can be arbitrarily enhanced by extending the number of the voltage multiplier (VM) stages and phases, respectively. The experimental results of a 350-W prototype demonstrated that in addition to the automatic current balancing capability, step-up conversion ratios could be arbitrarily changed by extending the VM stages.**

Keywords—Automatic current balancing, boost converter, high extendibility, high step-up converter, interleaved converter.

I. INTRODUCTION

Increasing concerns over global warming and the depletion of fossil fuels have been driving vigorous research and development efforts on alternative energy sources with low carbon emissions. Among them are photovoltaic (PV) panels and fuel-cells that have been gaining considerable attention. Fig. 1 shows a typical grid-connected renewable energy system. In this system, the 400 V DC bus is installed so as to be connected to the grid via the inverter. In general, since PV panels and fuel-cells are low-voltage energy sources (c.a., 20–40 V), high step-up boost converters are necessary to step up these voltages to 400 V. In addition, these boost converters should be capable of large input currents because of the huge voltage gap between their input and output.

Interleaved converters [1]–[4], [12]–[14] consisting of parallel-connected multiple converters have been widely employed for large input current applications. These converters operating out of phase at the same frequency can reduce the current ripples of the input and output ports and enhance the current capacity. Gain characteristics of parallel-connected phases are imbalanced to some extent due to minor mismatches among phases, such as duty cycles d and component tolerances. Inductor currents (hereafter call 'phase current') are imbalanced due to the mismatched gain
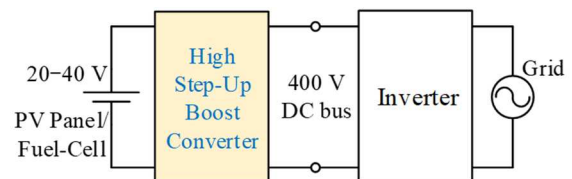

Fig. 1. Typical grid-connected renewable energy system.

characteristics, resulting in the current concentration and the increased current stresses of components. Phase currents of traditional interleaved converters are balanced by actively adjusting d of each phase so as to match the gain characteristics. This current balancing method, however, needs additional feedback control loops and current sensors, increasing the system complexity and cost [1].

Interleaved converters with an automatic current balancing capability have been proposed to reduce the system complexity and cost [2]–[4]. Although the magnetic coupling technique achieves the automatic phase current balancing [2], an increased circuit volume due to additional bulky magnetic components is cited as a top concern. The automatic current balancing techniques based on the charge conservation of capacitors have also been proposed [3], [4]. In addition to the reduced circuit volume compared to [2], these techniques can arbitrarily extend the number of phases without impairing the automatic current balancing capability.

Meanwhile, the voltage stresses of switches and diodes of conventional boost converters [1] are equal to a full output voltage V_{out}. In general, switches' on-resistance is proportional to the 2.2–2.6th power of its breakdown voltage, and hence resistances of high voltage switches are prone to soar. The higher the voltage stresses of diodes, the higher will be the forward-voltage drop. Consequently, high voltage stresses of switches and diodes tend to lower power conversion efficiencies of converters.

The conventional boost converters [1] with a voltage conversion ratio of $V_{out}/V_{in} = 1/(1-d)$ (where V_{in} is an input voltage) must operate with extremely high duty cycles (i.e., $d \geq 0.90$) to step up 20–40 V input voltage to 400 V bus voltage. The extreme duty cycle operations increase current ripples, current stresses of components, and losses.

High step-up converters using coupled-inductors [5]–[9], and switched capacitor structures [10]–[14] reportedly realize high voltage conversion ratios with avoiding extreme duty cycle operations. Coupled-inductors can arbitrarily change voltage conversion ratios by adjusting these turns ratio [5]–[9].

These topologies, however, face challenges of the increased design difficulty of integrated magnetics and a poor extendibility. Meanwhile, switched capacitors [10]–[14] improve design flexibility and circuit extendibility because their conversion ratios can be arbitrarily changed by adding a voltage multiplier (VM) consisting of capacitors and diodes.

The two-phase interleaved switched capacitor converters [12]–[14] not only achieve an automatic current balancing but also arbitrarily enhance their step-up conversion ratios by adding the VM stages. However, their phase currents cannot be balanced depending on the number of VM stages. The modified topology [13] can reduce capacitor voltage stresses, but semiconductor voltage stresses are prone to increase, resulting in lower efficiency under heavy load conditions than that of [12]. Furthermore, the input and output ports of this converter do not share the same ground [13], likely limiting its applications. A topology in [14], on the other hand, can arbitrarily enhance the current capacity and the step-up conversion ratio by extending the number of phases and VM stages, respectively. However, since capacitor voltage stresses soar as the number of VM stages increases, the converter needs to be redesigned with properly selecting capacitors depending on applications, impairing the extendibility.

This paper proposes a highly extendable interleaved high step-up boost converter with an automatic current balancing and reduced voltage stresses of semiconductors. The proposed converter is derived from a combination of an interleaved boost converter and VM stages. Phase currents are automatically balanced without feedback control loops nor current sensors due to the charge conservation of capacitors, achieving the reduced system complexity and cost by eliminating the feedback control loop. In addition, the current capacity and step-up conversion ratio of the proposed converter can be arbitrarily enhanced by extending the number of phases and VM stages, respectively. Thanks to the enhanced design flexibility, the proposed converter can be applied to various kinds of low-voltage large-current renewable energy sources.

The rest of this paper is organized as follows. Section II presents the circuit description and discusses the extendibility of the proposed converter. Section III explains the detailed operation analysis. Quantitative comparisons of various topologies will be performed in Section IV, followed by the experimental verification based on a 350-W prototype in Section V.

II. PROPOSED INTERLEAVED BOOST CONVERTERS

A. Circuit Description

Fig. 2 shows three typical examples of proposed interleaved boost converters. The proposed ones consist of multiple phases and VM stages. In the three-phase three-stage (3p-3s) topology in Fig. 2(a), for example, Phase A comprises components with a subscript 'A', and the first stage consists of components with subscript '1' (i.e., D_{A1}–D_{C1} C_{A1}–C_{C1}).

The number of stages and phases can be arbitrarily changed to obtain desired step-up conversion ratios and current capacities, respectively, as will be discussed in Section II-C. Extended topologies are exemplified in Figs. 2(b) and (c). Extending phases and stages enhance current capacities and step-up conversion ratios, respectively, allowing the proposed converters to flexibly be adopted to renewable energy sources.
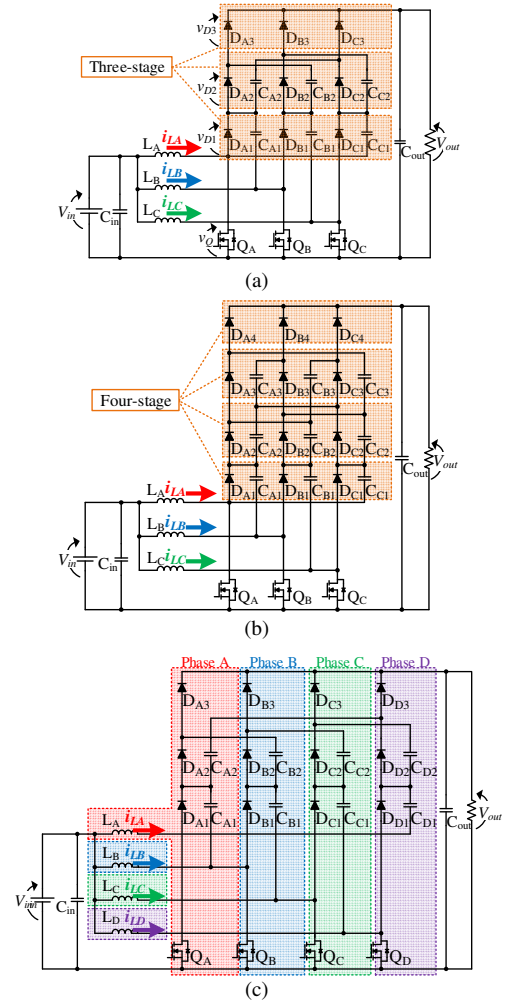

Fig. 2. Proposed interleaved boost converters: (a) 3p-3s, (b) 3p-4s, and (c) 4p-3s topologies.

B. Features

Except for the input and output smoothing capacitors, C_{in} and C_{out}, all capacitors in the VM are charged to $V_{in}/(1-d)$, as will be discussed in Section III-A. Therefore, a step-up conversion ratio of the 3p-3s topology is $3/(1-d)$, which is triple that of conventional interleaved boost converters [1]. The higher step-up conversion allows to avoid extreme duty cycle operations and to reduce current ripples, current stresses of components, and losses. Section III-B will discuss the detailed analysis of the conversion ratios.

Voltage stresses of switches and diodes in the conventional interleaved boost converters [1] are equal to V_{out}. In the proposed converter, on the other hand, the voltage stresses can be reduced lower than two-thirds of V_{out} thanks to C_{A1}–C_{C1} and C_{A2}–C_{C2}. The reduced voltage stresses of switches and diodes translate to low on-resistance and low forward-voltage, respectively. Theoretical voltage stresses of the switches and diodes will be analyzed in Section III-C.

Regardless of mismatch in d and component tolerances among phases, the phase current i_{Lj} (where j is A, B, or C) can be automatically balanced thanks to the charge conservation of C_{A1}–C_{C1} and C_{A2}–C_{C2}. In other words, no additional feedback control loops nor current sensors are necessary for current balancing, reducing the system complexity and cost by eliminating the current balancing feedback control loop. Section III-D will explain the current balancing mechanism.
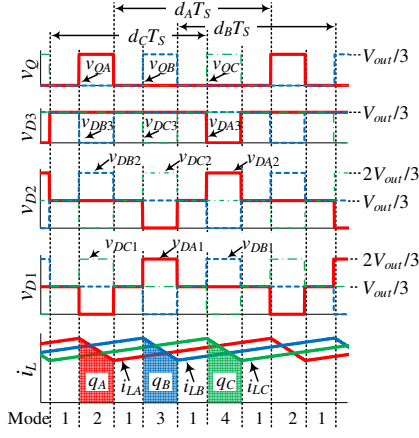
Fig. 3. Theoretical key waveforms.

C. Extendibility

Step-up conversion ratios of the proposed converters can be arbitrarily enhanced by extending VM stages. In comparison with the 3p-3s topology in Fig. 2(a), a step-up conversion ratio of the 3p-4s topology in Fig. 2(b) is enhanced to be $4/(1-d)$ due to the increased number of the VM stage. A step-up conversion ratio of a converter with M stages can be generalized as $M/(1-d)$.

The proposed converters can arbitrarily change its current capacities by extending the number of phases. The current capacity of the 4p-3s topology in Fig. 2(c), for example, can process larger current than does the 3p-3s topology because of the increased number of phases connected in parallel.

In summary, the proposed converters can adjust step-up conversion ratios and current capacities by extending the VM stages and phases, respectively. Hence, thanks to the design flexibility, the proposed converter can be applied to renewable energy sources with low-voltage large-current characteristics.

III. OPERATION ANALYSIS

In this section, the operation analysis is performed for the 3p-3s topology. Three switches Q_A–Q_C operate with an interleaving manner 120° out of phase, and d of Q_A–Q_C must be larger than 0.33 for the interleaving operation and automatic current balancing. Operation principles vary depending on whether a duty cycle condition falls into $0.33 < d < 0.67$ or $0.67 \leq d < 1$. The operation analysis is performed only for the case of $0.67 \leq d < 1$, due to the page limitation.

The theoretical key operation waveforms and current flows are shown in Figs. 3 and 4, respectively. v_Q is the drain-source voltage of switches, v_{D1}–v_{D3} are voltages of diodes. d_A–d_C are duty cycles of Q_A–Q_C, q_A–q_C are the amounts of the charge stored in capacitors with subscripts 'A', 'B', and 'C', respectively, and T_S is the switching period. Capacitances of C_{A1}–C_{C1} and C_{A2}–C_{C2} are assumed large enough, and their voltages are constant. Forward-voltages of diodes are neglected to simplify the analysis.

A. Operational Mode Analysis and Current Flows

The operation modes are divided into four based on switching states.

Mode 1 [Fig. 4(a)]: Q_A–Q_C are on. The input voltage V_{in} is applied to L_A–L_C, and the phase currents of i_{LA}–i_{LC} linearly increase. All diodes are reversed biased and do not conduct. C_{out} supplies the current to the load.
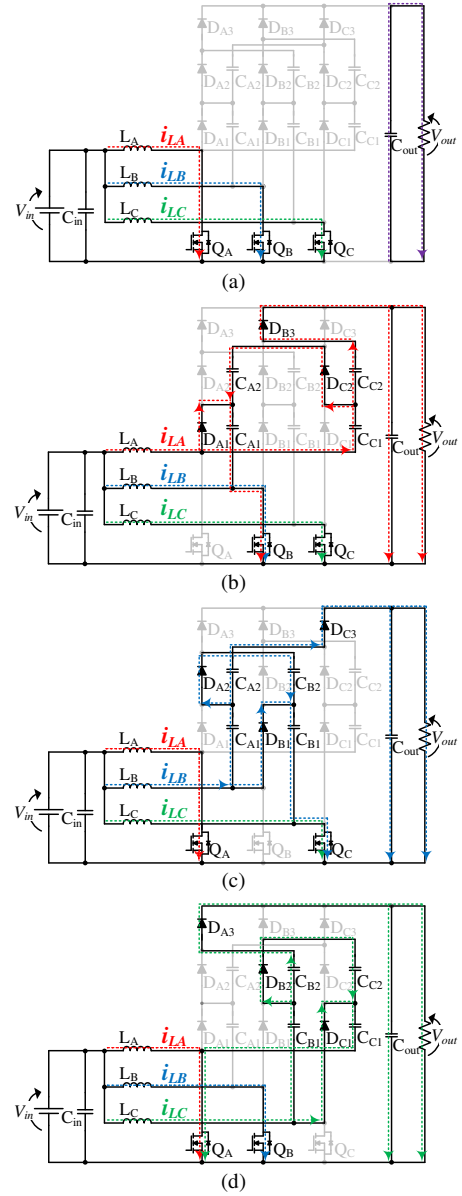

Fig. 4. Current flows of the 3p-3s topology in (a) Mode 1, (b) Mode 2, (c) Mode 3, and (d) Mode 4.

Mode 2 [Fig. 4(b)]: Q_B and Q_C are still on, and Q_A is turned off. i_{LB} and i_{LC} still linearly increase, whereas i_{LA} starts decreasing. D_{A1}, D_{B3}, and D_{C2} are forward biased, and i_{LA} charges C_{A1} and C_{A2}, and discharges C_{C1} and C_{C2}.

Mode 3 [Fig. 4(c)]: Q_B is off, Q_A and Q_C are on. L_B discharges, and its current i_{LB} linearly decreases. D_{A2}, D_{B1}, and D_{C3} are forward biased. i_{LB} charges C_{B1} and C_{B2}, and discharges C_{A1} and C_{A2}.

Mode 4 [Fig. 4(d)]: Q_C is off, and Q_A and Q_B are on. i_{LC} linearly decreases. D_{A3}, D_{B2}, and D_{C1} are forward biased, and i_{LC} charges C_{C1} and C_{C2}, and discharges C_{B1} and C_{B2}.

When one of three switches is off, C_{A1}–C_{C1}, and C_{A2}–C_{C2} charge or discharge. As shown in Fig. 3, off periods of Q_A–Q_C are $(1-d_A)T_S$, $(1-d_B)T_S$, and $(1-d_C)T_S$, respectively. The volt-sec balance on L_A–L_C yields the following equation

$$d_j T_S V_{in} + (1 - d_j) T_S (V_{in} - V_{Cj1}) = 0 \qquad (1)$$

where j is A, B, or C, and V_{CA1}–V_{CC1} are the voltages of C_{A1}–C_{C1}, respectively. Rearrangement of (1) yields

$$V_{Cj1} = \frac{V_{in}}{1 - d_j}. \qquad (2)$$

The voltages of C_{A2}–C_{C2}, V_{CA2}–V_{CC2}, are derived by applying the volt-sec balances on L_A–L_C, respectively. From the Kirchhoff's voltage law at Mode 2–4, V_{CA2}–V_{CC2} are

$$V_{Cj2} = V_{Cl1} - V_{Cj1} + \frac{V_{in}}{1 - d_j}$$

$$= \frac{V_{in}}{1 - d_l} \quad (l = C, A, B) \qquad (3)$$

where l is C when j is A.

In summary, given that all duty cycles are identical as $d_A = d_B = d_C = d$, (2), and (3) can be generalized as

$$V_{Cjn} = \frac{V_{in}}{1 - d} \quad (n = 1, 2). \qquad (4)$$

B. *Step-Up Conversion Ratio*

This section derives step-up conversion ratios of the 3p–3s and 3p–4s topologies, and finally generalize for the *M* stage topology. All the circuit elements are assumed to be ideal, and all duty cycles d_A–d_C are equal to d.

As shown in Fig. 4, drain-source voltages of Q_A–Q_C (i.e., v_{QA}–v_{QC}) are equivalent to V_{CA1}–V_{CC1}, respectively. The following equation is derived by (4), as

$$v_{Qj} = \frac{V_{in}}{1 - d}. \qquad (5)$$

V_{out} of the 3p-3s topology can be derived from the sum of voltages of switches and VM capacitors. V_{out} in Mode 2 [see Fig. 4(b)], for example, is the sum of v_{QA}, V_{CC1}, and V_{CC2}. V_{out} in Modes 3 and 4 can be obtained similarly. Combining (4) and (5) yields the following equation,

$$V_{out} = v_{Qj} + V_{Cl1} + V_{Cl2} = \frac{3V_{in}}{1 - d} \qquad (6)$$

Thus, a step-up conversion ratio of the 3p-3s topology is three times higher than that of the conventional boost converters [1].

The larger the number of VM stages, the higher will be the step-up conversion ratios. Thanks to the increase in VM stages, V_{out} of 3p-4s topology in Fig. 2(b) is enhanced to be

$$V_{out} = v_{Qj} + V_{Cl1} + V_{Cl2} + V_{Cl3} = \frac{4V_{in}}{1 - d} \qquad (7)$$

where V_{CA3}–V_{CC3} are the voltages of third-stage capacitors (i.e., C_{A3}–C_{C3}). Thus, V_{out} of the topology with the *M* stage VM is generalized as

$$V_{out} = v_{Qj} + V_{Cl1} + V_{Cl2} + \cdots + V_{Cl(M-1)}$$

$$= \frac{MV_{in}}{1 - d}. \qquad (8)$$

This equation suggests that the proposed converter can arbitrarily change step-up conversion ratios by adjusting *M*.

C. *Voltage Stresses of Switches and Diodes*

This section derives the maximum voltage stresses of switches and diodes in the 3p-3s and 3p-4s topologies. All the circuit elements are assumed to be ideal, and thus all duty cycles d_A–d_C are equal to d.

From (4) and (5), v_{QA}–v_{QC} in the 3p-3s topology are equivalent to V_{CA1}–V_{CC1}, respectively, and thus v_{Qj} is reduced lower than one-third of V_{out}. V_{out} determines the voltages of diodes (i.e., v_{DA1}–v_{DC1}, v_{DA2}–v_{DC2}, and v_{DA3}–v_{DC3}), V_{CA1}–V_{CC1}, and V_{CA2}–V_{CC2}. v_{DA1}, for example, is the sum of V_{CB1} and V_{CB2}

[see Fig. 4(c)]. v_{DA2} and v_{DA3} are the subtraction of V_{CA1} from V_{out}, and of V_{CB1} and V_{CB2} from V_{out} [see Figs. 4(d), and (b)], respectively. Combining (4) and (6) yields

$$v_{Dj1} = V_{Ck1} + V_{Ck2} = \frac{2V_{in}}{1 - d} \quad (k = B, C, A) \qquad (9)$$

$$v_{Dj2} = V_{out} - V_{Cj1} = \frac{2V_{in}}{1 - d} \qquad (10)$$

$$v_{Dj3} = V_{out} - (V_{Ck1} + V_{Ck2}) = \frac{V_{in}}{1 - d} \qquad (11)$$

where k is B when j is A.

Hence, combining (5), (6), and (9)–(11), the voltages of D_{A1}–D_{C1}, D_{A2}–D_{C2}, and Q_A–Q_C, D_{A3}–D_{C3} in the 3p-3s topology are reduced lower than two-thirds and one-third of V_{out}, respectively.

Although detailed derivation is omitted due to the page limitation, the maximum voltage stresses in the 3p-4s topology can be derived similarly to those of the 3p-3s topology. From (5) and (7), v_{Qj} is lower than one-fourth of V_{out}. v_{Dj1} is given by (9), and v_{Dj2}, v_{Dj3}, and the voltages of D_{A4}–D_{C4}, v_{DA4}–v_{DC4}, are

$$v_{Dj2} = V_{Cl1} + V_{Cl2} + V_{Cl3} - V_{Cj1} = \frac{2V_{in}}{1 - d} \qquad (12)$$

$$v_{Dj3} = V_{out} - (V_{Cj1} + V_{Cj2}) = \frac{2V_{in}}{1 - d} \qquad (13)$$

$$v_{Dj4} = V_{out} - (V_{Cl1} + V_{Cl2} + V_{Cl3}) = \frac{V_{in}}{1 - d}. \qquad (14)$$

From (5), (7), (9), and (12)–(14), the voltages of D_{A1}–D_{C1}, D_{A2}–D_{C2}, D_{A3}–D_{C3}, and Q_A–Q_C, D_{A4}–D_{C4} in the 3p-4s topology are reduced lower than one-half and one-fourth of V_{out}, respectively.

The voltage stresses of switches and diodes in the proposed converters can be reduced lower than two-thirds of V_{out}, whereas those in the traditional converter are V_{out}. The more the number of VM stages, the lower will be the voltage stresses of switches and diodes. Hence, low-voltage semiconductor devices with low on-resistance and low forward-voltage can be used.

D. *Current Balancing Mechanism*

In the proposed converters, the phase current i_{Lj} can be automatically balanced thanks to the charge conservation of VM capacitors. This section demonstrates the current balancing mechanism using charge vector analysis [15] based on Kirchhoff's current law. This analysis is applied to derive the unique amounts of charge in the 3p-3s topology. To simplify the analysis, L_A–L_C are treated as constant current sources. Mode 1 is irrelevant to current balancing and therefore is omitted. d_A–d_C are assumed equal to d.

Fig. 5 illustrates the equivalent circuits and charge flows in Modes 2–4. Diodes and switches in the equivalent circuits are omitted to simplify them. I_{LA}–I_{LC}, and q_{A1}–q_{C1}, q_{A2}–q_{C2} are defined as the averaged phase currents and the amounts of the charge delivered via C_{A1}–C_{C1} and C_{A2}–C_{C2}, respectively. I_{out} is an output current, and R is a load resistance. Applying the Kirchhoff's current law at nodes a–f yields

$$\begin{cases} 0 = q_A - q_{A1} + q_{A2} - q_{C1} \\ 0 = -q_{A2} + q_{C1} - q_{C2} \\ 0 = q_{A1} - q_{A2} - q_{B2} \\ 0 = q_B - q_{A1} - q_{B1} + q_{B2} \\ 0 = q_{B1} - q_{B2} - q_{C2} \\ 0 = q_C - q_{B1} - q_{C1} + q_{C2} \end{cases} \qquad (15)$$
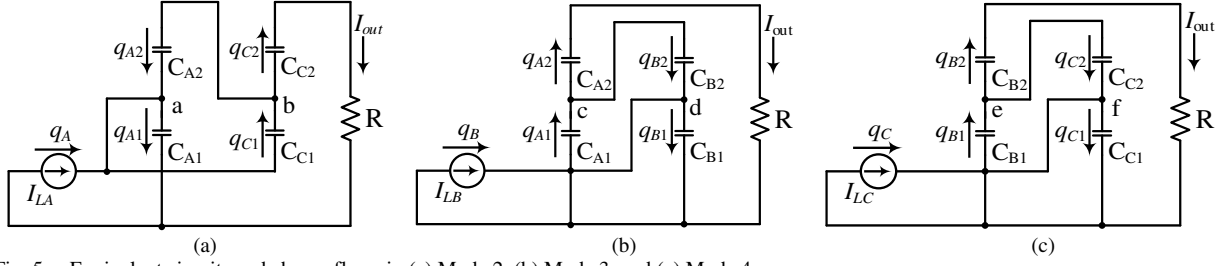
Fig. 5. Equivalent circuits and charge flows in (a) Mode 2, (b) Mode 3, and (c) Mode 4.

Assuming that the load is a constant current source, $q_{A2} = q_{B2} = q_{C2}$, yielding

$$\begin{cases} 0 = q_{A2} - q_{B2} \\ 0 = q_{A2} - q_{C2} \end{cases} \quad (16)$$

I_{out} is defined as

$$I_{out} = q_{A2} + q_{B2} + q_{C2} \quad (17)$$

Combining (15)–(17) yields

$$\begin{bmatrix} 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ I_{out} \end{bmatrix} = \begin{bmatrix} 1 & 0 & 0 & -1 & 1 & 0 & 0 & -1 & 0 \\ 0 & 0 & 0 & 0 & -1 & 0 & 0 & 1 & -1 \\ 0 & 0 & 0 & 1 & -1 & 0 & -1 & 0 & 0 \\ 0 & 1 & 0 & -1 & 0 & -1 & 1 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 1 & -1 & 0 & -1 \\ 0 & 0 & 1 & 0 & 0 & -1 & 0 & -1 & 1 \\ 0 & 0 & 0 & 0 & 1 & 0 & -1 & 0 & 0 \\ 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 & -1 \\ 0 & 0 & 0 & 0 & 1 & 0 & 1 & 0 & 1 \end{bmatrix} \begin{bmatrix} q_A \\ q_B \\ q_C \\ q_{A1} \\ q_{A2} \\ q_{B1} \\ q_{B2} \\ q_{C1} \\ q_{C2} \end{bmatrix} \quad (18)$$

Providing I_{out} with (18) yields all amounts of charges depicted in Fig. 5. Applying $I_{out} = 3$ into (18), for example, yields $[q_A, q_B, q_C, q_{A1}, q_{A2}, q_{B1}, q_{B2}, q_{C1}, q_{C2}]^T = [3, 3, 3, 2, 1, 2, 1, 2, 1]^T$, and therefore, q_A–q_C are equal.

The amount of charge can be converted into the current by the following equation

$$I_{Lj} = \frac{q_j}{1 - d}. \quad (19)$$

From (18), q_A–q_C are equal, and hence, I_{LA}–I_{LC} are matched. Thus, i_{Lj} can be automatically balanced thanks to the charge conservation of C_{A1}–C_{C1} and C_{A2}–C_{C2}.

If all the circuit components are ideal, I_{LA}–I_{LC} are completely matched. In the actual circuits, however, I_{LA}–I_{LC} are slightly imbalanced due to the mismatched d and component tolerances among phases. When the off periods of Q_A–Q_C [see Fig. 3] are $(1-d_A)T_s$, $(1-d_B)T_s$, and $(1-d_C)T_s$, respectively, the following equation is

$$q_j = (1 - d_j)T_s I_{Lj}. \quad (20)$$

According to (18), q_A–q_C are equal, and therefore, the following equation is given by using (20), as

$$(1 - d_A)T_s I_{LA} = (1 - d_B)T_s I_{LB} = (1 - d_C)T_s I_{LC} \quad (21)$$

If all duty cycles are identical, the averaged phase currents can be generalized as I_L. Given that d_A–d_C are mismatched as $d_A = d-\Delta d$, and $d_B = d_C = d$, I_{LB} and I_{LC} can be balanced as I_L, where Δd is an error in d due to the non-ideality of microcontrollers and gate drives. (21) can be rewritten as

$$(1 - d + \Delta d)I_{LA} = (1 - d)I_L \quad (22)$$

Rearrangement of (22) produces

$$\frac{I_{LA}}{I_L} = \frac{1 - d}{1 - d + \Delta d}. \quad (23)$$

(23) represents the degree of the phase current imbalance because of the error Δd. To verify the automatic current balancing capability, d_A is assumed to be intentionally severely mismatched to d. Applying $\Delta d = 0.01$ and $d = 0.82$ into (23) yields approximately equal to 0.95, implying the 5% imbalance between I_{LA} and I_L. The phase currents of the conventional converters cannot be balanced under the same degree of the mismatched d, resulting in the extreme current concentration. On the other hand, the phase currents of the proposed converter are balanced with the error of merely 5%. Thus, the phase currents of the proposed one can be automatically balanced despite the severely mismatched d.

Component tolerances, such as inductances, on-resistances of switches, and forward-voltages of diodes, cause a slight imbalance of the phase currents. If inductances are mismatched, the peak phase currents are imbalanced. Meanwhile, the averaged phase currents are not imbalanced because voltages of parallel-connected inductors are equal. If on-resistances of switches or forward-voltages of diodes are mismatched, voltages of inductors are not equal due to the mismatch in the voltage drop of switches and diodes, resulting in the phase currents to be slightly imbalanced. This current imbalance would be minor enough compared to the phase current imbalance caused by the mismatched d, and can be neglected. Therefore, component tolerances no longer affect the current balancing capability in the proposed converter.

In summary, thanks to the charge conservation of the VM capacitors, the phase current i_{Lj} can be automatically balanced regardless of the mismatched d and component tolerances among phases. Hence, additional feedback control loops and current sensors are not needed for current balancing, reducing the system complexity and cost.

IV. QUANTITATIVE COMPARISON OF VARIOUS TOPOLOGIES

A. Total Device Power Rating

Total Device Power Rating (TDPR) is used as an index to quantitatively compare different topologies from the viewpoint of semiconductor volt-amp stresses [16]. TDPR is the sum of maximum volt-amp stresses of all semiconductor devices normalized by the input or output power and is defined as

$$TDPR = \sum_{\substack{ALL\ MOSFETs \\ ALL\ DIODEs}} \frac{V_{max}I_{max}}{V_{in}I_{in}} \left(= \frac{V_{max}I_{max}}{V_{out}I_{out}}\right) \quad (24)$$

where V_{max} and I_{max} are the maximum voltage and current stresses, respectively, and I_{in} is an input current. In general, the lower value of TDPR, the lower will be the power conversion losses [16]. Currents flowing through switches and diodes are constant to simplify the analysis. d_A–d_C and I_{LA}–I_{LC} are equal to d and I_L, respectively.

Table I illustrates the maximum volt-amp stresses of switches and diodes in the proposed converters. This section

derives only the maximum volt-amp stresses in the 3p-3s topology due to the page limitation. The maximum voltage stresses of switches and diodes can be obtained, as described in Section III-C. All diode currents are automatically balanced thanks to the charge conservation of VM capacitors. In addition to the demonstration of this balancing mechanism, the maximum current stresses of switches and diodes are derived by using charge vector analysis [15]. As shown in Figs 4(a), and 5(a), when I_{out} is 3, the charge flows into D_{A1} and D_{C2} are derived from (18), as

$$q_A - q_{C1} = 1 \qquad (25)$$
$$q_{C1} - q_{C2} = 1. \qquad (26)$$

The charge flow into D_{B3} is equivalent to the charge delivered via C_{C2}. From (18), (25), and (26), the charge flows into D_{A1}, D_{C2}, and D_{B3} are equal, and therefore, their currents are balanced as $I_L/3$. Their maximum current stresses are $I_{in}/9$ because I_L is $I_{in}/3$. As the current flowing through Q_B is equivalent to those through D_{A1}, D_{C2}, and Phase B, the maximum current stress of Q_B is $5/9I_{in}$. Although the detailed derivation is omitted due to the page limitation, those of all switches and diodes can be obtained similarly.

B. TDPRs of Various Topologies

TDPRs of the proposed converters and the conventional converter [1] are compared in Fig. 6. *TDPRs* of the proposed ones are lower than that of the conventional one at a given step-up conversion ratio. Thanks to the reduced volt-amp stresses of all semiconductor devices, the proposed ones can reduce *TDPRs* as the number of VM stages increases. Meanwhile, when topologies with the stages are the same (e.g., the 3p-3s and 4p-3s), *TDPRs* of these topologies are equal. These results mean the number of phases is irrelevant to *TDPR*. Therefore, phase numbers of the proposed ones should be determined by desired current capacities.

V. EXPERIMENTAL RESULTS

A. Prototype

Fig. 7. illustrates a photograph of a 350-W prototype for the 3p-4s topology. The component values of the prototype are listed in Table II. The number of VM stages in the prototype can be arbitrarily changed up to the four stages. The prototype was designed for V_{in} = 24 V, V_{out} = 400 V, and the switching frequency was 100 kHz.

B. Measured Waveforms

The measured key waveforms in the 3p-3s topology at the full load of 350-W are shown in Fig. 8. These waveforms were in good agreement with the theoretical ones shown in Fig. 3. The prototype demonstrated that the voltages of switches and diodes were suppressed to less than two-thirds of the output voltage, and the phase currents were automatically balanced.

C. Automatic Current Balancing

Based on the measured waveforms of i_{LA}–i_{LC} in the 3p-3s topology, the averaged phase currents I_{LA}–I_{LC} were calculated from the following equation

$$I_{Lj} = \frac{1}{T_S} \int_0^{T_S} i_{Lj} dt \qquad (27)$$

Fig. 9 shows the calculated I_{LA}–I_{LC}. I_{LA}–I_{LC} were precisely balanced with errors less than 2% over the output power range. Hence, i_{LA}–i_{LC} were automatically balanced regardless of the mismatched d and component tolerances.

TABLE I
MAXIMUM VOLT-AMP STRESSES OF THE PROPOSED CONVERTERS

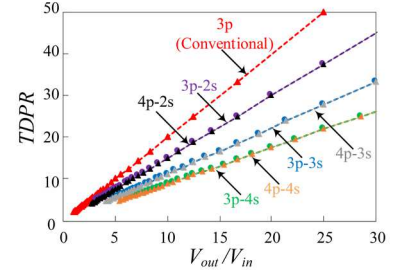|		Components				
		Q_j	D_{j1}	D_{j2}	D_{j3}	D_{j4}
3p-2s	V_{max}	$V_{in}/(1-d)$	$2V_{in}/(1-d)$	$V_{in}/(1-d)$		
	I_{max}	$I_{in}/2$	$I_{in}/6$	$I_{in}/6$		
4p-2s	V_{max}	$V_{in}/(1-d)$	$2V_{in}/(1-d)$	$V_{in}/(1-d)$		
	I_{max}	$3I_{in}/8$	$I_{in}/8$	$I_{in}/8$		
3p-3s	V_{max}	$V_{in}/(1-d)$	$2V_{in}/(1-d)$	$2V_{in}/(1-d)$	$V_{in}/(1-d)$	
	I_{max}	$5I_{in}/9$	$I_{in}/9$	$I_{in}/9$	$I_{in}/9$	
4p-3s	V_{max}	$V_{in}/(1-d)$	$2V_{in}/(1-d)$	$2V_{in}/(1-d)$	$V_{in}/(1-d)$	
	I_{max}	$5I_{in}/12$	$I_{in}/12$	$I_{in}/12$	$I_{in}/12$	
3p-4s	V_{max}	$V_{in}/(1-d)$	$2V_{in}/(1-d)$	$2V_{in}/(1-d)$	$2V_{in}/(1-d)$	$V_{in}/(1-d)$
	I_{max}	$7I_{in}/12$	$I_{in}/12$	$I_{in}/12$	$I_{in}/12$	$I_{in}/12$
4p-4s	V_{max}	$V_{in}/(1-d)$	$2V_{in}/(1-d)$	$2V_{in}/(1-d)$	$2V_{in}/(1-d)$	$V_{in}/(1-d)$
	I_{max}	$7I_{in}/16$	$I_{in}/16$	$I_{in}/16$	$I_{in}/16$	$I_{in}/16$

Fig. 6. *TDPRs* as a function of step-up conversion ratios.
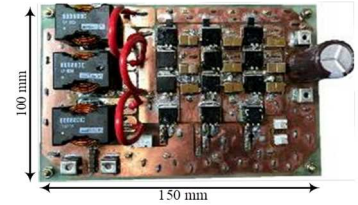

Fig. 7. Photograph of 350-W prototype for the 3p-4s topology.

TABLE II
COMPONENT VALUES OF THE PROTOTYPE

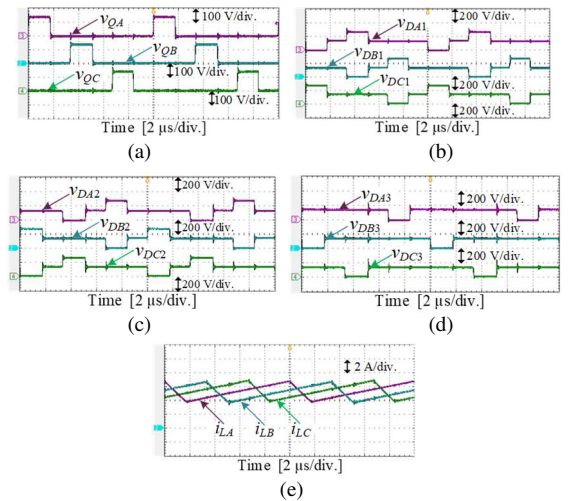| Components	Value
Switches	MOSFET, STB57N65M5, R_{on} = 63 mΩ
L_A–L_C	Inductor, 60B683C, 68 μH
C_{A1}–C_{C3}	Ceramic Capacitor, 2.2 μF × 4
D_{A1}–D_{C3}	Schottky Diode, SCS212AJ, V_F = 1.35 V
D_{A4}–D_{C4}	Schottky Diode, STPS2200, V_F = 0.58 V
C_{in}	Ceramic Capacitor, 10 μF × 5
C_{out}	Aluminum Electrolytic Capacitor, 100 μF

Fig. 8. Measured key waveforms: (a) v_{QA}–v_{QC}, (b) v_{DA1}–v_{DC1}, (c) v_{DA2}–v_{DC2}, (d) v_{DA3}–v_{DC3}, and (e) i_{LA}–i_{LC}.

D. Output Characteristics

Fig. 10 shows the output characteristics of the 3p-3s and 3p-4s topologies and the conventional boost converters [1]. Step-up conversion ratios of the 3p-3s and 3p-4s topologies were three and four times higher than that of the conventional ones, respectively. The proposed converter could arbitrarily change step-up conversion ratios by extending the VM stages.

E. Power Conversion Efficiency

The measured power conversion efficiencies of the 3p-3s topology and [13] are compared in Fig.11. In the 3p-3s topology, the peak efficiency at 220-W was as high as 92.89%. The efficiency of the 3p-3s topology was higher than that of [13] under heavy load conditions because semiconductor volt-amp stresses are lower than [13].

VI. CONCLUSION

This paper has proposed the highly extendable interleaved high step-up boost converter for renewable energy systems. The proposed converter achieves the automatic current balancing and the reduced semiconductor voltage stresses. The number of VM stages and phases can be arbitrarily enhanced to obtain desired step-up conversion ratios and current capacities, respectively.

The quantitative result verified *TDPRs* of the proposed converters are lower than that of the conventional converter at the given step-up conversion ratio. The experimental results demonstrated the phase currents were automatically balanced, and the step-up conversion ratios could be arbitrarily changed by extending the VM stage.

Our future works include loss analysis and development of higher power conversion efficiency.
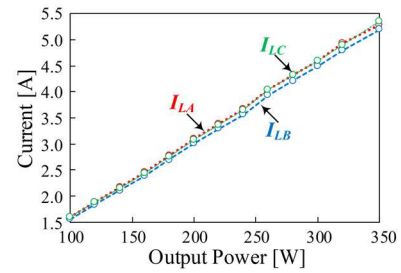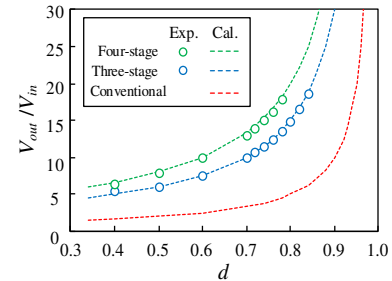

Fig. 9.   Measured phase currents.

Fig. 10.   Experimental and theoretical step-up conversion ratios.

Fig. 11.   Measured power conversion efficiency curve of the 3p-3s topology and that of [13].

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